NL17SZU04

Single Unbuffered Inverter

The NL17SZU04 is a single unbuffered inverter in two tiny footprint package. The device performs much as LCX multi−gate products in speed and drive.

Features

- Tiny SOT−353 and SOT−553 Packages
- Source/Sink ± 16 mA at 4.5 V V_{CC}
- Over−Voltage Tolerant Inputs and Outputs
- Pin For Pin with NC7SZU04P5X, TC7SZU04FU and TC7SZU04AFE
- Chip Complexity: FETs = 20
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Pb−Free Packages are Available

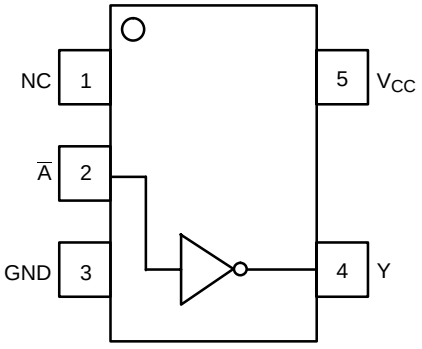


Figure 1. Pinout (Top View)

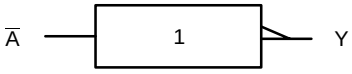
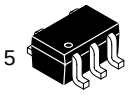


Figure 2. Logic Symbol

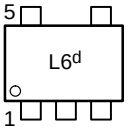
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MARKING DIAGRAMS



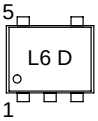
SOT−353/SC70−5/SC−88A
DF SUFFIX
CASE 419A



d = Date Code



SOT−553
XV5 SUFFIX
CASE 463B



L6 = Device Marking
D = One Digit Date Code

PIN ASSIGNMENT

Pin	Function
1	NC
2	$\overline{A}$
3	GND
4	Y
5	V_{CC}

FUNCTION TABLE

Input	Output $Y = \overline{A}$
A	**Y**
L	H
H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	DC Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage		−0.5 to +7.0	V
I_{IK}	DC Input Diode Current		−50	mA
I_{OK}	DC Output Diode Current		−50	mA
I_{OUT}	DC Output Sink Current		±50	mA
I_{CC}	DC Supply Current per Supply Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance	SOT−353 (Note 1) SOT−553	350 496	°C/W
P_D	Power Dissipation in Still Air at 85°C	SOT−353 SOT−553	186 135	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	Class IC Class A N/A	V

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2−ounce copper trace with no air flow.
2. Tested to EIA/JESD22−A114−A, rated to EIA/JESD22−A114−B.
3. Tested to EIA/JESD22−A115−A, rated to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage	(Operating) Data Retention Only	1.65 1.5	5.5 5.5	V
V_{IN}	DC Input Voltage		0	5.5	V
V_{OUT}	DC Output Voltage		0	5.5	V
T_A	Operating Temperature Range		−40	+85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.0 V ±0.3 V V_{CC} = 5.0 V ±0.5 V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			−40°C ≤ T_A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High−Level Input Voltage		1.65 to 1.85	0.85 V_{CC}			0.85 V_{CC}		V
			2.3 to 5.5	0.8 V_{CC}			0.8 V_{CC}		
V_{IL}	Low−Level Input Voltage		1.65 to 1.85			0.15 V_{CC}		0.15 V_{CC}	V
			2.3 to 5.5			0.2 V_{CC}		0.2 V_{CC}	
V_{OH}	High−Level Output Voltage V_{IN} = V_{IL} or V_{IH}	I_{OH} = −100 μA I_{OH} = −3 mA	1.65 to 5.5 1.65	V_{CC} − 0.1 1.29	V_{CC} 1.52		V_{CC} − 0.1 1.29		V
		I_{OH} = −4 mA	2.3	1.9	2.1		1.9		
		I_{OH} = −6 mA	2.7	2.2	2.4		2.2		
		I_{OH} = −8 mA	3.0	2.4	2.7		2.4		
		I_{OH} = −12 mA	3.0	2.3	2.5		2.3		
		I_{OH} = −16 mA	4.5	3.8	4.0		3.8		
V_{OL}	Low−Level Output Voltage V_{IN} = V_{IH} or V_{OH}	I_{OL} = 100 μA I_{OL} = 3 mA	1.65 to 5.5 1.65		 0.08	0.1 0.24		0.1 0.24	V
		I_{OL} = 4 mA	2.3		0.20	0.3		0.3	
		I_{OL} = 6 mA	2.7		0.22	0.4		0.4	
		I_{OL} = 8 mA	3.0		0.28	0.4		0.4	
		I_{OL} = 12 mA	3.0		0.38	0.55		0.55	
		I_{OL} = 16 mA	4.5		0.42	0.55		0.55	
I_{IN}	Input Leakage Current	V_{IN} = V_{CC} or GND	0 to 5.5			±0.1		±1.0	μA
I_{OFF}	Power Off−Output Leakage Current	V_{OUT} = 5.5 V	0			1		10	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	1.65 to 5.5			1		10	μA

AC ELECTRICAL CHARACTERISTICS $t_R = t_F$ = 3.0 ns

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C		−40°C ≤ T_A ≤ 85°C		Unit
				Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay (Figure 3 and 4)	R_L = 1 MΩ, C_L = 15 pF	1.8 ± 0.15	1.0	11.7	1.0	12.1	ns
		R_L = 1 MΩ, C_L = 15 pF	2.5 ± 0.2	0.8	6.2	0.8	6.5	
		R_L = 1 MΩ, C_L = 15 pF	3.3 ± 0.3	0.5	4.5	0.5	4.8	
		R_L = 500 Ω, C_L = 50 pF		1.0	6.0	1.0	6.5	
		R_L = 1 MΩ, C_L = 15 pF	5.0 ± 0.5	0.5	3.9	0.5	1.0	
		R_L = 500 Ω, C_L = 50 pF		0.8	5.0	0.8	5.5	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	4.5	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	10 MHz, V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	6.5	pF
		10 MHz, V_{CC} = 5.5 V, V_I = 0 V or V_{CC}	10	

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

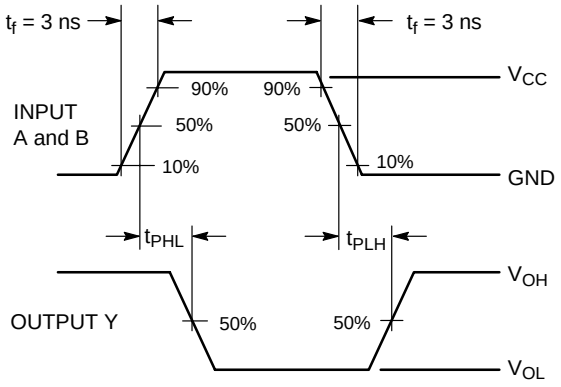
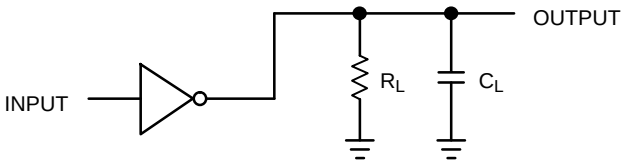


Figure 3. Switching Waveform



A 1−MHz square input wave is recommended for propagation delay tests.

Figure 4. Test Circuit

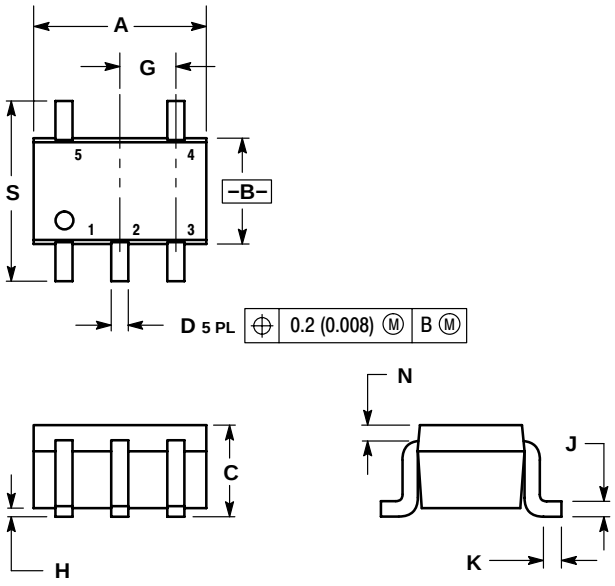
DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature							Package Type	Tape and Reel Size†
	Logic Circuit Indicator	No. of Gates per Package	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape and Reel Suffix		
NL17SZU04DFT2	NL	1	7	SZ	U04	DF	T2	SOT−353/ SC70−5/ SC−88A	178 mm, 3000 Unit
NL17SZU04DFT2G	NL	1	7	SZ	U04	DF	T2	SOT−353/ SC70−5/ SC−88A (Pb−Free)	178 mm, 3000 Unit
NL17SZU04XV5T2	NL	1	7	SZ	U04	XV5	T2	SOT−553*	178 mm, 4000 Unit

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*All Devices in Package SOT553 are Inherently Pb−Free.

PACKAGE DIMENSIONS

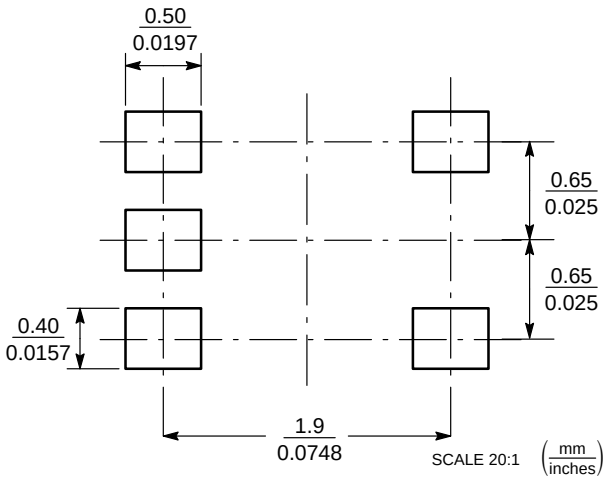
SOT−353
DF SUFFIX
5−LEAD PACKAGE
CASE 419A−02
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

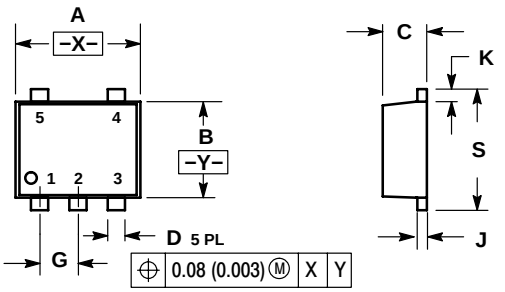
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SOT−553
XV5 SUFFIX
5−LEAD PACKAGE
CASE 463B−01
ISSUE A



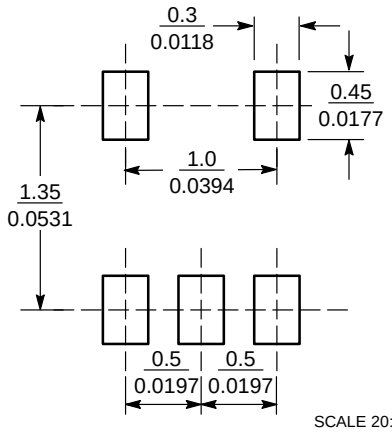
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.50	1.70	0.059	0.067
B	1.10	1.30	0.043	0.051
C	0.50	0.60	0.020	0.024
D	0.17	0.27	0.007	0.011
G	0.50 BSC		0.020 BSC	
J	0.08	0.18	0.003	0.007
K	0.10	0.30	0.004	0.012
S	1.50	1.70	0.059	0.067

STYLE 1:
PIN 1. BASE 1
2. EMITTER 1/2
3. BASE 2
4. COLLECTOR 2
5. COLLECTOR 1

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE

SOLDERING FOOTPRINT*



SCALE 20:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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