

256K x 16高速异步 具有3.3V电源的CMOS静态RAM

2011年12月

特征

- 高速访问时间：
-10,12ns
- CMOS低功耗
- 低功耗：
-Less than 5mA (典型值) CMOS排列
- TTL兼容的接口级别
- 单个3.3V电源供应
- 完全静止操作：no clock or refresh 需要
- 三态输出
- Data control for upper and lower bytes
- 工业温度可用
- 无铅可用

描述

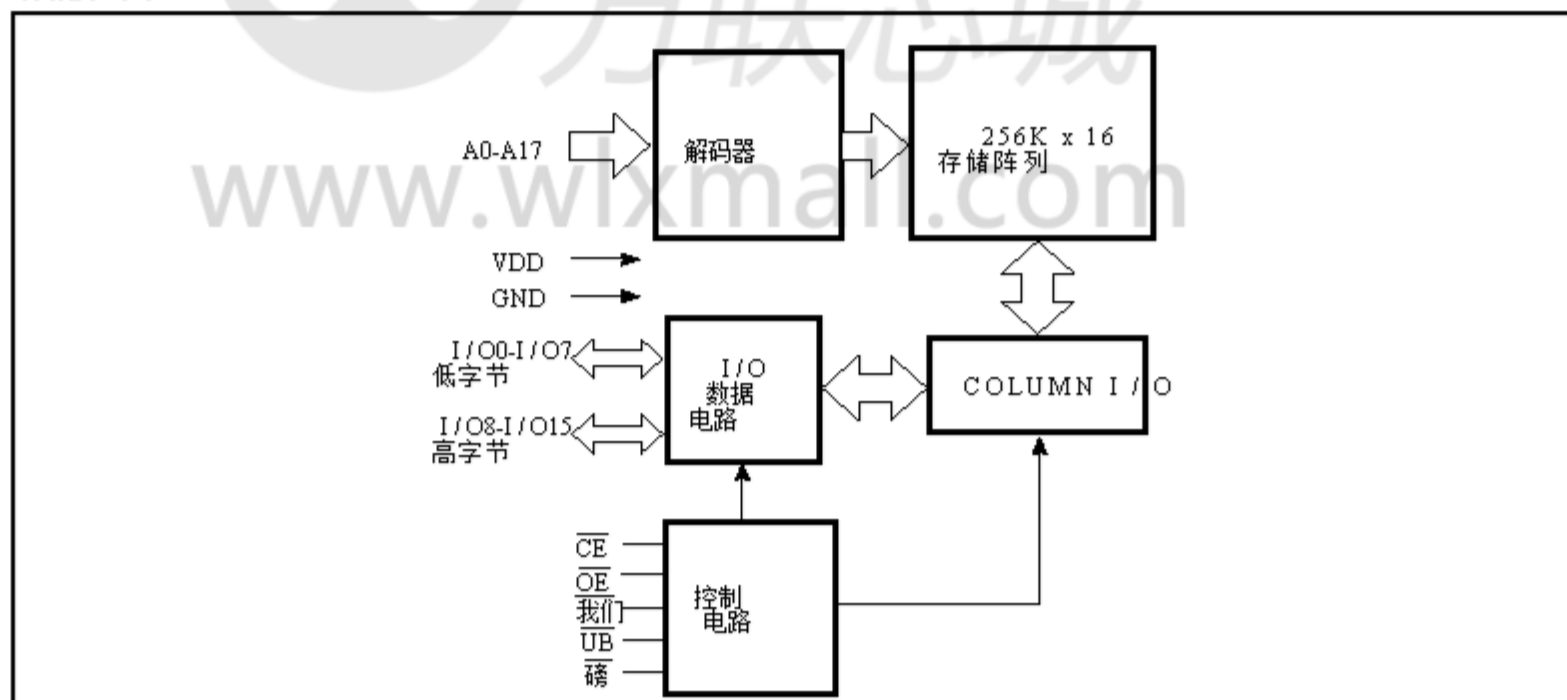
该 ISSI IS61LV25616AL is a high-speed, 4,194,304位 static RAM organized as 262,144 words by 16 bits. It is fabricated using ISSI's high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yield high-performance and low power consumption devices.

当CE为高电平（取消选择）时，器件假定为standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, CE and OE. The active LOW Write Enable (WE) controls both writing and reading of the memory. A data byte allows Upper Byte (UB) and Lower Byte (LB) of the access.

The IS61LV25616AL is packaged in the JEDEC standard 44 pin 400-mil SOJ, 44-pin TSOP Type II, 44 pin LQFP and 48-pin MiniBGA (8mm x 10mm).

功能框图



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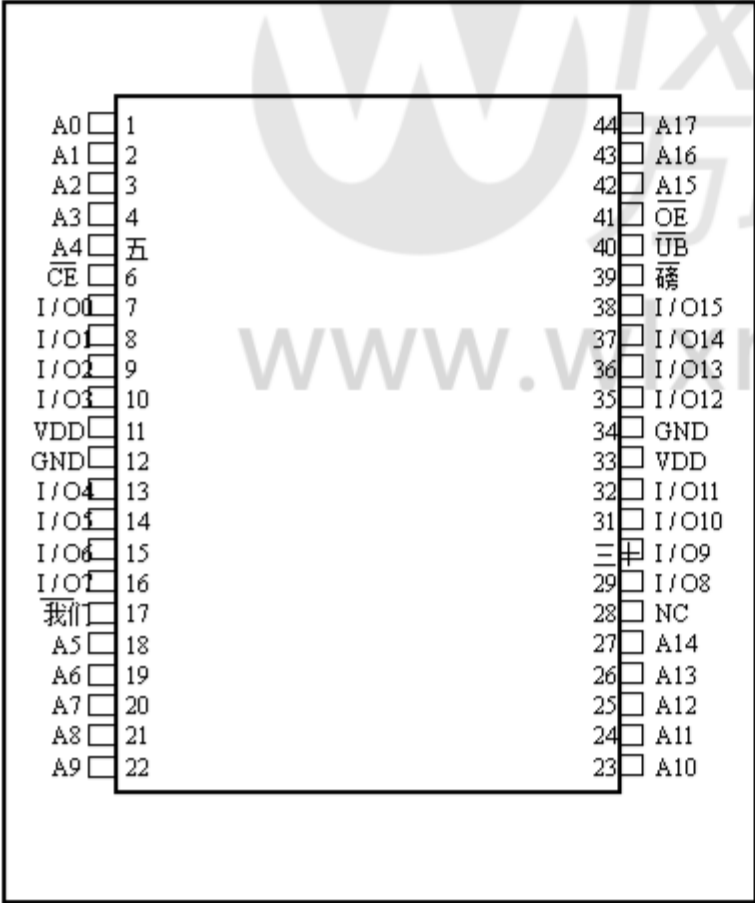
- the risk of injury or damage has been minimized;
- the user assumes all such risks; and
- potential liability of Integrated Silicon Solution, Inc. is adequately protected under the circumstances.

真理表

模式	我们	CE	OE	磅	UB	I / O PIN		V DD 电流
						I / 00-I / 07	I / 08-I / 015	
未选中的	X	H	X	X	X	高-Z	高-Z	我 sb 1，我 sb 2
OutputDisabled	H	大号	H	X	X	高-Z	高-Z	我 cc
	X	大号	X	H	H	高-Z	高-Z	
读	H	大号	大号	大号	H	D 出来	高-Z	我 cc
	H	大号	大号	H	大号	高-Z	D 出来	
	H	大号	大号	大号	大号	D 出来	D 出来	
写	大号	大号	X	大号	H	D In	高-Z	我 cc
	大号	大号	X	H	大号	高-Z	D In	
	大号	大号	X	大号	大号	D In	D In	

引脚配置

44引脚TSOP（类型II）和SOJ

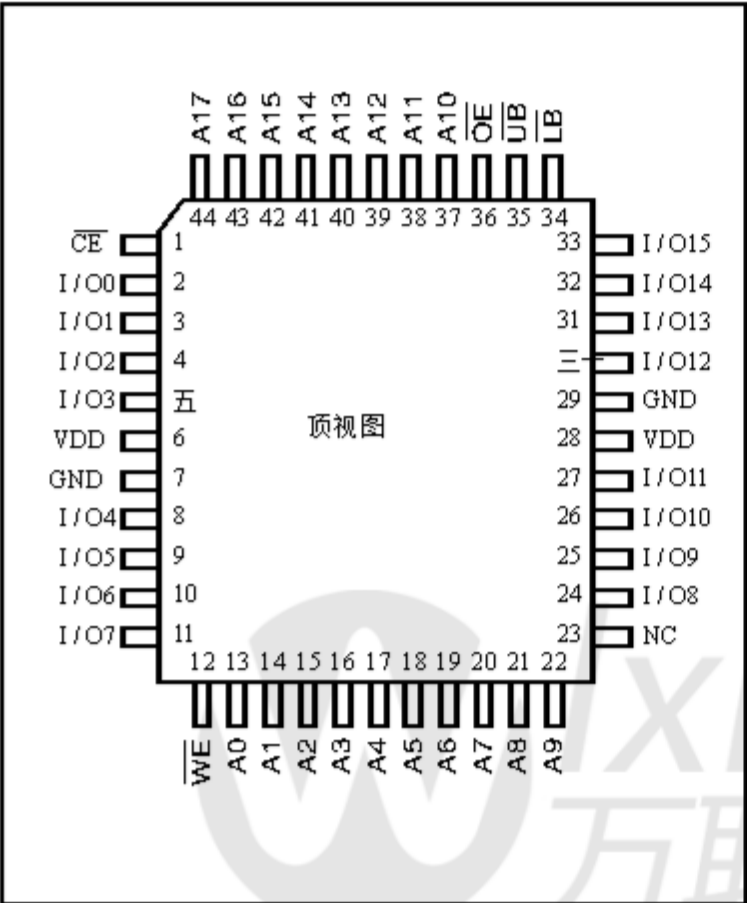


引脚说明

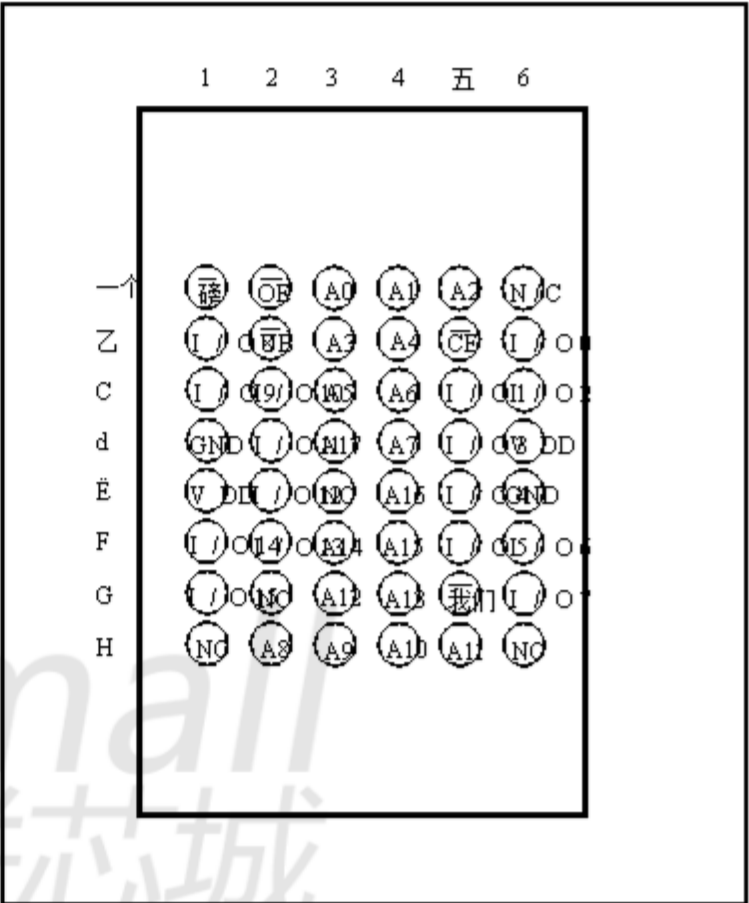
A0-A17	AddressInputs
I / 00-I / 015	DataInputs / 输出
CE	ChipEnableInput
OE	OutputEnableInput
我们	WriteEnableInput
磅	低byteControl (I / 00-I / 07)
UB	上层byteControl (I / 08-I / 015)
NC	无连接
V DD	功率
GND	地面

引脚配置

44引脚LQFP



48引脚小型BGA



引脚说明

A0-A17	AddressInputs
I/O0-I/O15	DataInputs /输出
CE	ChipEnableInput
OE	OutputEnableInput
我们	WriteEnableInput
磅	低byteControl (I/O0-I/O7)
UB	上层byteControl (I/O8-I/O15)
NC	无连接
V DD	功率
GND	地面

绝对最大额定值 (1)

符号参数	值	单元	
V 期限	TerminalVoltagewithRespecttoGND	-0.5toV DD +0.5	V
t stg	储存温度	-65to + 150	C
P t	功耗	1.0	w ^

注意:

1. 由于ABSOLUTE MAXIMUM RATINGS可能导致应力下降
 permanent damage to the device. This is a stress rating only and functional operation
 of the device at these or any other conditions above those indicated in the operational
 本规范的部分内容不作任何暗示. 暴露于绝对最大额定值
 conditions for extended periods may affect reliability.

工作范围

范围	环境温度	V _{DD} 为10ns	为12ns
广告	0°C TO +70°C	3.3V + 10%, -5%	3.3V + 10%
产业	-40°C TO +85°C	3.3V + 10%, -5%	3.3V + 10%

DC电气特性 (过压范围)

符号参数	测试条件	闲.	最大.	单元
V _{oH}	Output HIGH Voltage V _{DD} = Min., I _{oH} = -4.0mA	2.4	-	V
V _{oL}	Output LOW Voltage V _{DD} = 最小, I _{oL} = 8.0mA	-	0.4	V
V _{IH}	Input HIGH Voltage	2.0	V _{DD} + 0.3	V
V _{IL}	Input LOW Voltage (1)	-0.3	0.8	V
我李	Input Leakage GND ≤ V _I ≤ V _{DD}	COM. 工业.	-2 5	μA
我Lo	Output Leakage GND ≤ V _{out} ≤ V _{DD} Outputs Disabled	COM. 工业.	-2 5	μA

笔记:

1. V_{IL} (min.) = -2.0V, 脉冲宽度为10ns.

电源特性 (1) (OverOperatingRange)

符号参数	测试条件	-10 闭.最大.	-12 闭.最大.	单元
我 cc 电源电流	V DD =最大, COM. I out = 0 mA, f = f maX 工业.	- 100 - 110	- 90 - 100	嘛
我 某人 (TTLInputs)	V DD =最大, COM. V In = V IH 或 V IL 工业. CE ≥ V IH, f = f maX.	- 50 - 55	- 45 - 50	嘛
我 sb 1 (TTLInputs)	V DD =最大, COM. V In = V IH 或 V IL 工业. CE ≥ V IH, f = 0	- 20 - 25	- 20 - 25	嘛
我 sb 2 电流 (CMOSInputs)	V DD =最大, COM. CE ≥ V DD - 0.2V, 工业. V In ≥ V DD - 0.2V, 或 V In ≤ 0.2V, f = 0	- 15 - 20	- 15 - 20	嘛

注意:

1. At f = f maX, 地址和数据输入在最大频率上循环, f = 0意味着电流变化.
Shaded area product in development

电容 (1)

符号	参数	条件	最大.	单元
c	Input Capacitance	V In = 0V	6	pF的
c out	输入 / Output Capacitance	V out = 0V	8	pF的

注意:

1. 经过初步测试并进行了设计或处理, 以改变这些参数.

读周期切换特性 (1) (OverOperatingRange)

符号	参数	-10		-12		单元
		阅.最大.	阅.最大.	阅.最大.	阅.最大.	
t rc	ReadCycleTime	10	-	12	-	NS
t aa	AddressAccessTime	-	10	-	12	NS
你好	OutputHoldTime	2	-	2	-	NS
王牌	CE AccessTime	-	10	-	12	NS
t Doe	OE AccessTime	-	4	-	五	NS
t Hzoe (2)	OE toHigh-ZOutput	-	4	-	五	NS
t Lzoe (2)	OE 了tolow-ZOutput	0	-	0	-	NS
t Hzce (2)	CE toHigh-ZOutput	0	4	0	6	NS
t Lzce (2)	CE 了tolow-ZOutput	3	-	3	-	NS
t ba	磅, UBAccessTime	-	4	-	五	NS
t Hzb (2)	磅, UBtoHigh-ZOutput	0	3	0	4	NS
t Lzb (2)	磅, UBtoLow-ZOutput	0	-	0	-	NS
t Pu	PowerUpTime	0	-	0	-	NS
t PD	PowerDownTime	-	10	-	12	NS

笔记：

- 1, 测试条件: 假设信号转换时间为3ns, 时间参考电压1.5V, 输入脉冲电平0Vto3.0VandoutputloadingspecifiedinFigure1.
2.用负载测试图2.转换则里稳态电压±500mV.

AC测试负载

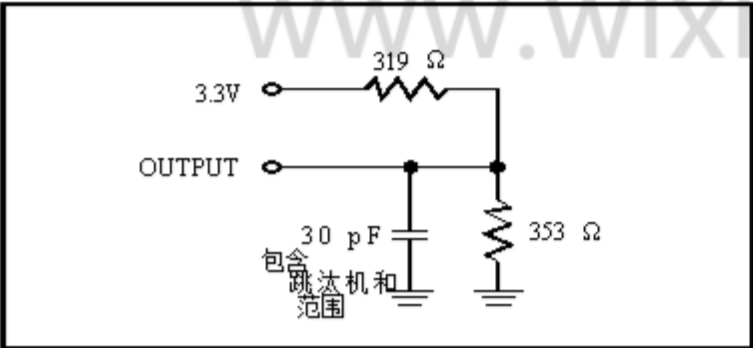


图1

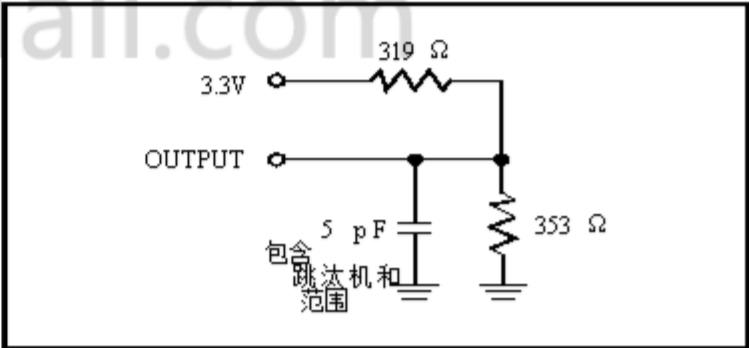
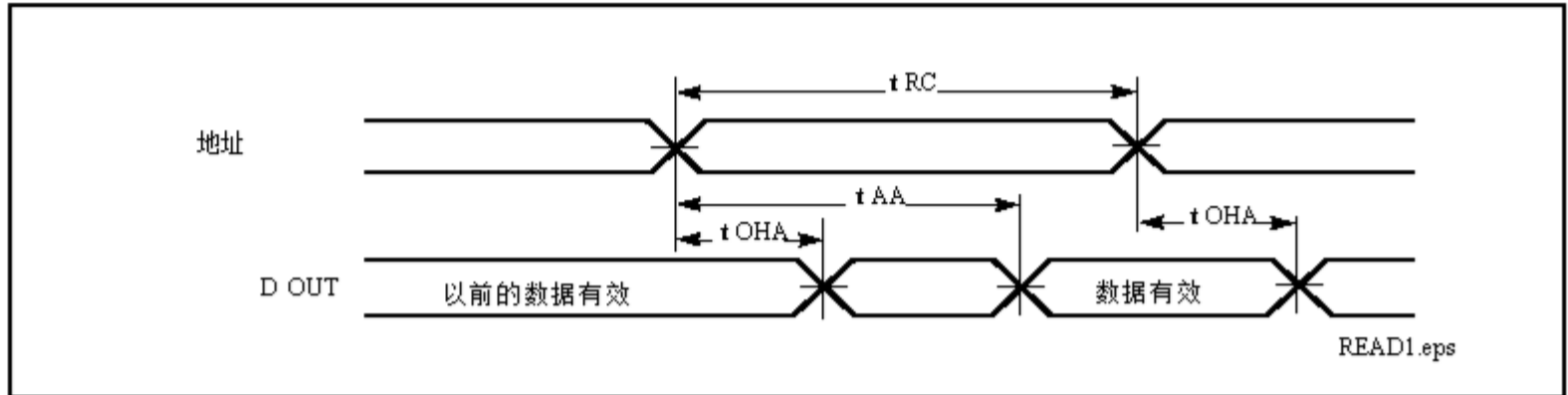


图2

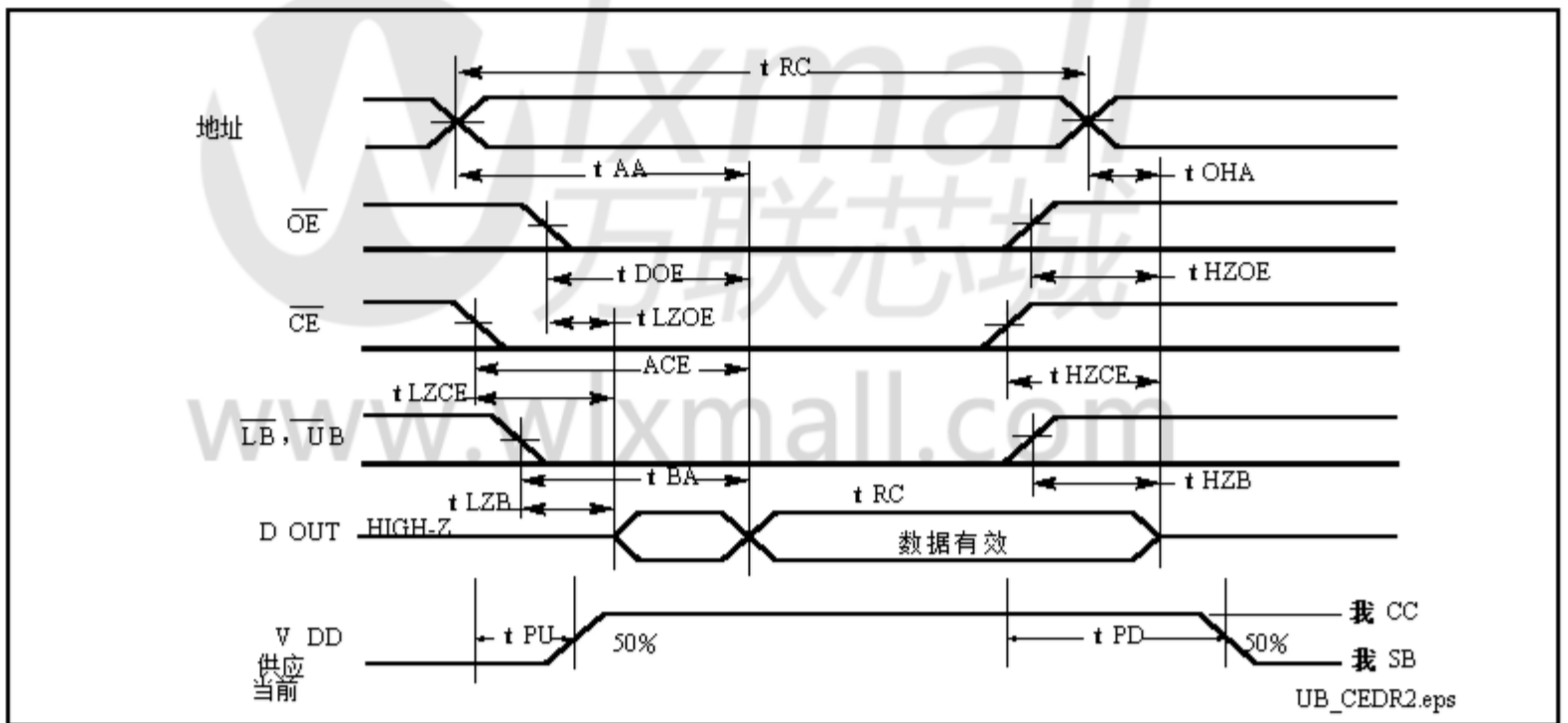
交流测试条件

参数	单元
InputPulseLevel	0Vto3.0V
InputRiseandFallTimes	为3ns
InputandOutputTimingandReferenceLevel	1.5V
OutputLoad	SeeFigures1and2

交流波形

阅读周期编号. 1 (1,2) (地址控制) ($CE = OE = V_{IL}$, UB 或 $LB = V_{IL}$)

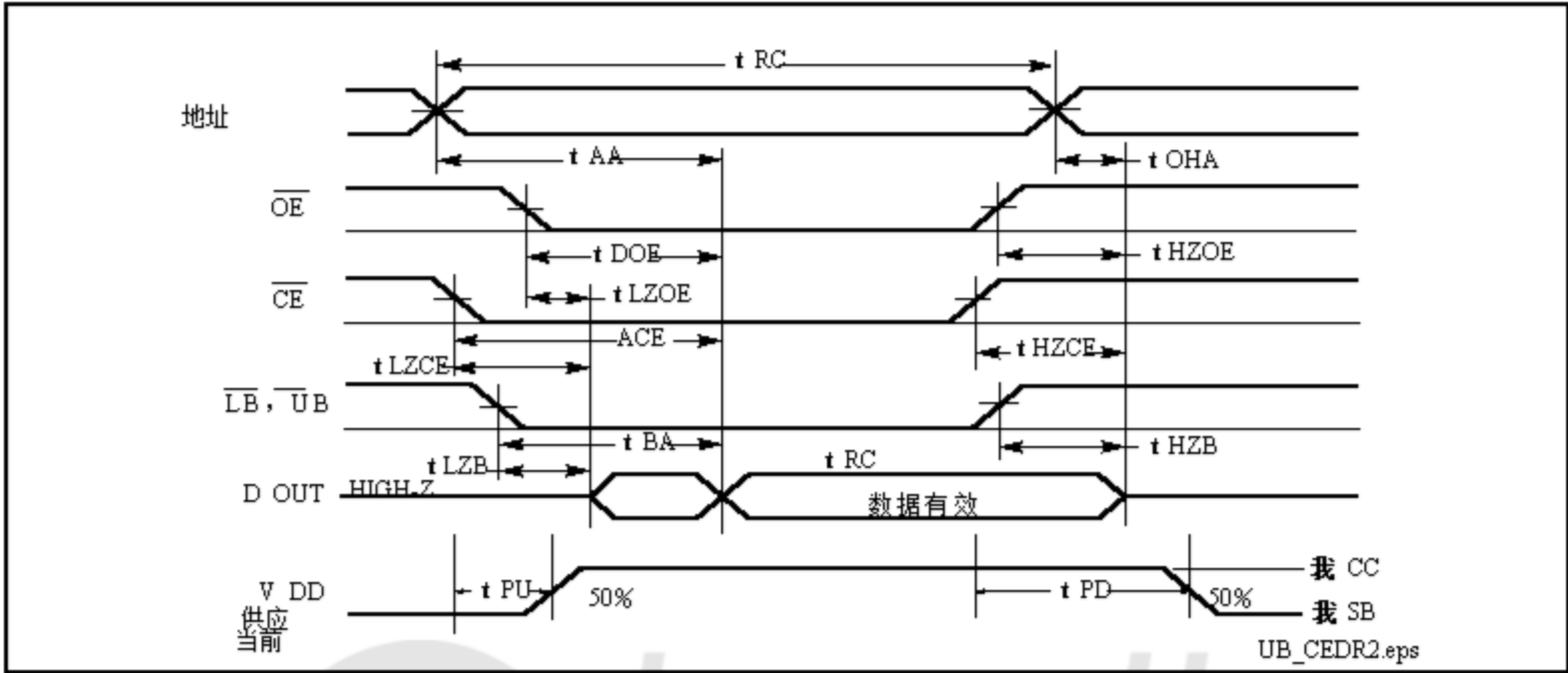
阅读周期编号. 2 (1,3)



笔记:

1. WE is High for a Read Cycle.
2. 设备连续选择. OE , CE , UB 或 $LB = V_{IL}$.
3. 地址无效, 与 CE LOW transition 同时发生.

阅读周期编号.2 (1,3)



- 笔记：
- 1. WEisHighforaReadCycle.
 - 2.设备连续选择.OE，CE，UB或LB = V IL.
 - 3.地址无效，与CELOWtransition同时发生.

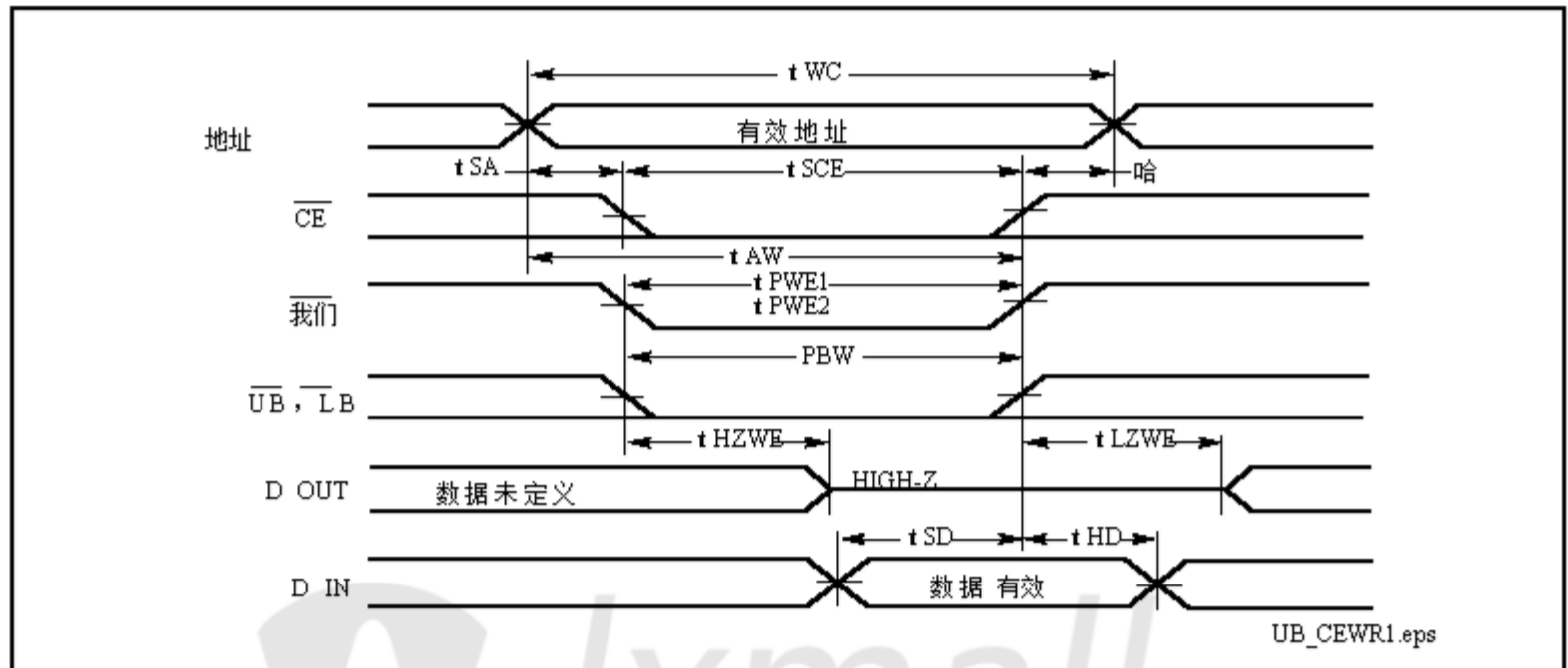
写周期切换特性 (1,3) (OverOperatingRange)

符号	参数	-10 阴.最大.	-12 阴.最大.	单元
t wc	WriteCycleTime	10	-	NS
t sce	CE toWriteEnd	8	-	NS
t aw	AddressSetupTimetoWriteEnd	8	-	NS
吨 哈	AddressHoldfromWriteEnd	0	-	NS
t sa	AddressSetupTime	0	-	NS
t Pwb	磅，UBValidtoEndofWrite	8	-	NS
t Pwe 1	我们脉冲宽度	8	-	NS
t Pwe 2	我们脉冲宽度 (OE = 低)	10	-	NS
t sD	DataSetuptoWriteEnd	6	-	NS
t HD	DataHoldfromWriteEnd	0	-	NS
t Hzwe (2)	我们LOWtoHigh-ZOutput	-	五	NS
t Lzwe (2)	我们HIGHtoLow-ZOutput	2	-	NS

- 笔记：
- 1，测试条件为3nsorless的信号转换时间，1.5V的时序参考电平，0V的输入脉冲电平 to3.0VandoutputloadingspecifiedinFigure1.
 - 2.用负载测试图2.转换测量±500mV的稳态电压.未测试100%.
 - 3.CELOW和UB或LB和WAOWOW的内容定义的内部写入时间无效.A信号必须无效 statestoinitiateaWrite，butanyonecangoinactive to terminate the Write.TheDataInputSetupandHoldtiming arereferencedtotherisingorfallingedgeofthesignalthatterminatesthewrite.

交流波形

WRITE CYCLE NO.1 (CE Controlled, OE is HIGH or LOW) (1)

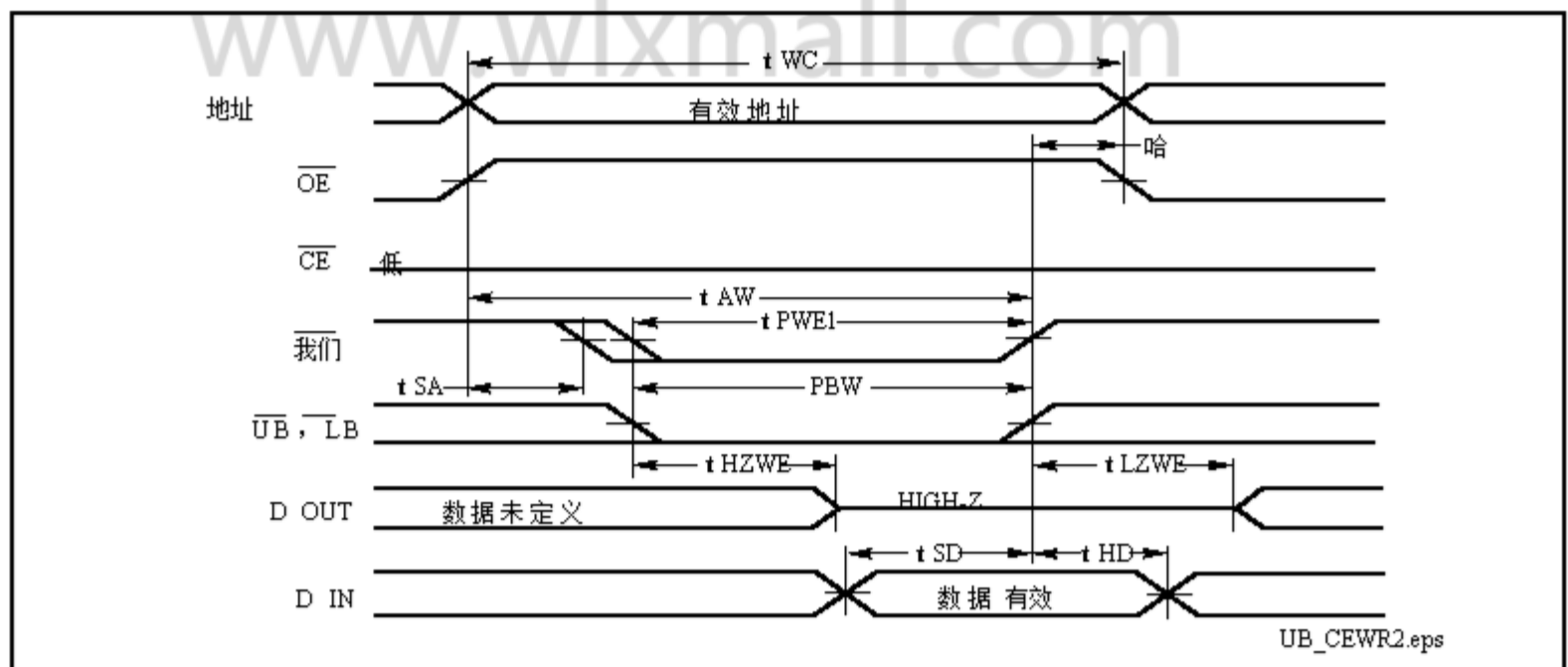


笔记:

WRITE在内部生成的信号在低于LOW的状态下表示CE和W输入和至少一个of the LB and UB inputs being in the LOW state.

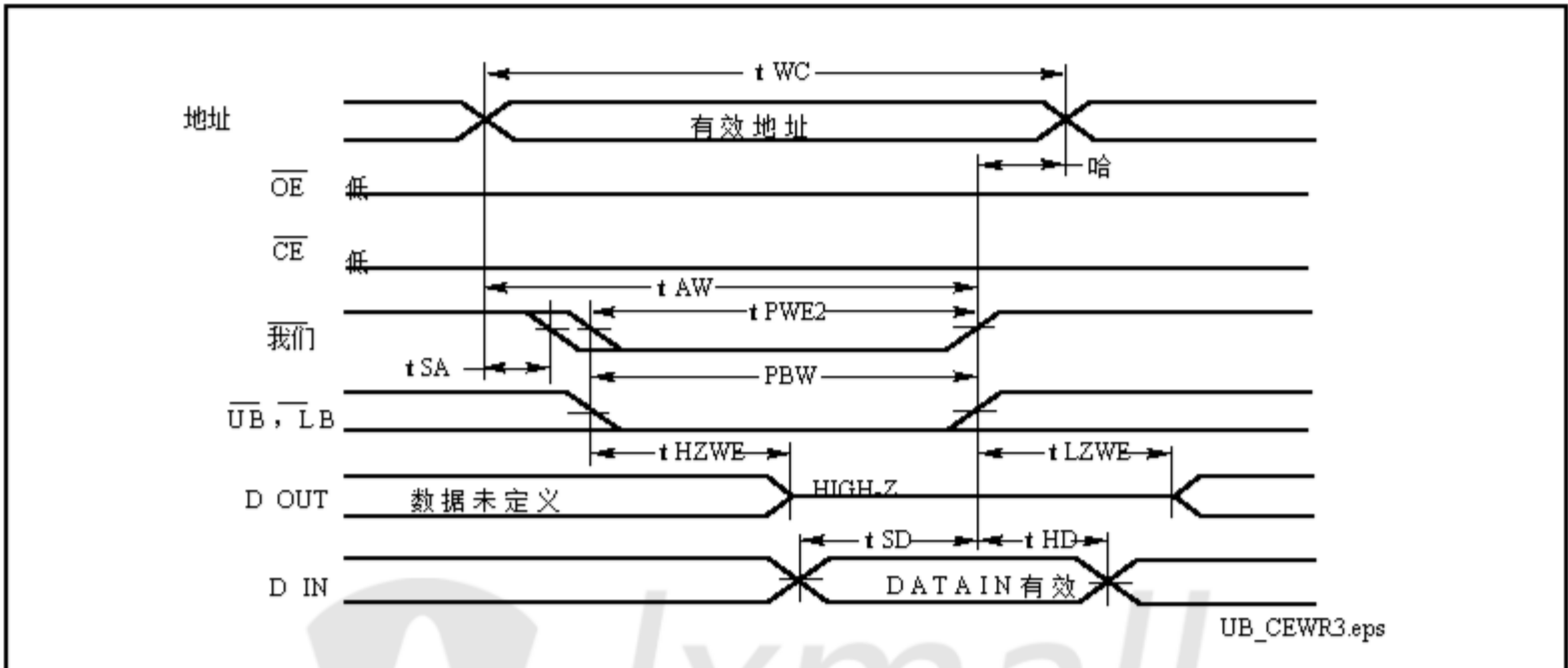
2. WRITE = (CE) [(LB) = (UB)] (WE).

WRITE CYCLE NO. 2 (WE Controlled, OE is High During Write Cycle) (1,2)

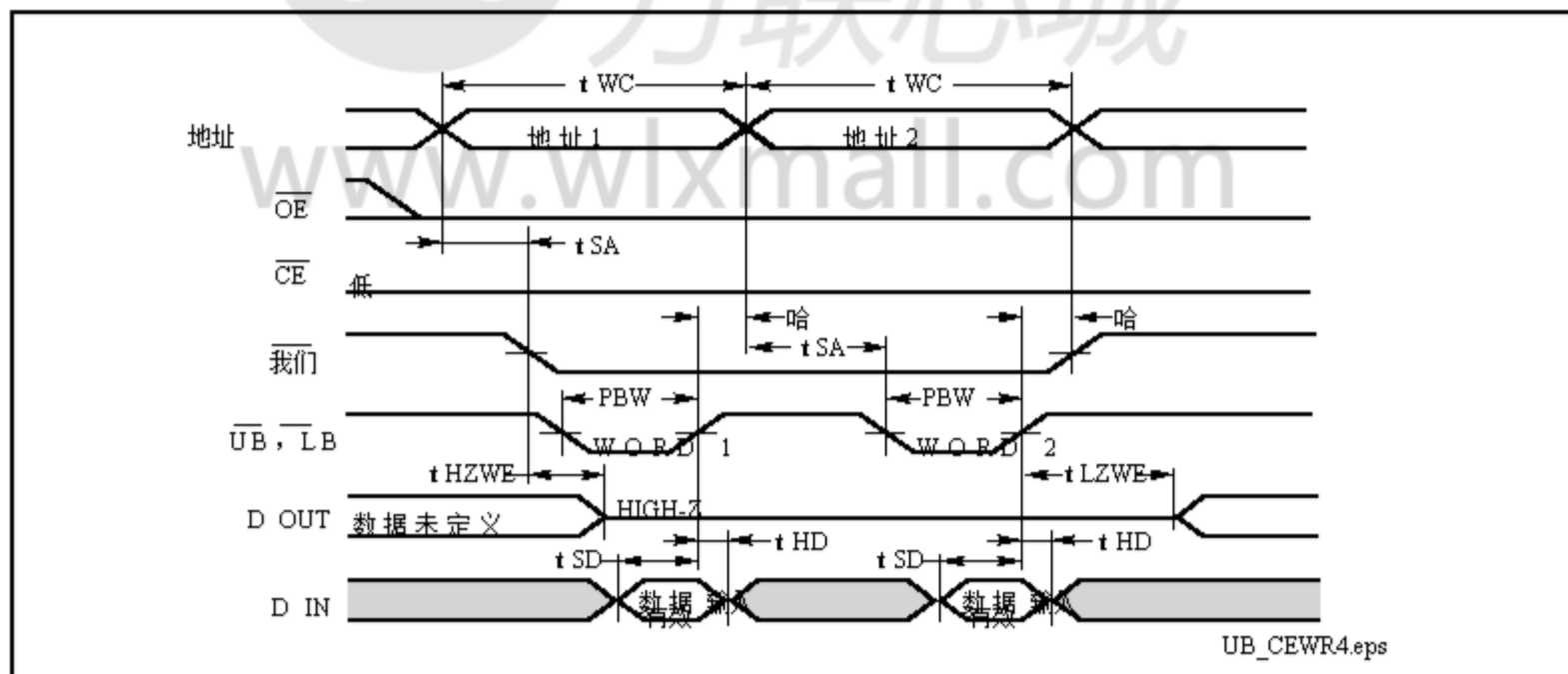


交流波形

WRITE CYCLE NO.3 (WE Controlled, OE is LOW During Write Cycle) (1)



WRITE CYCLE NO.4 (LB, UB控制, 背靠背写) (1,3)



笔记:

1. 内部写时间由CE = 低电平, UB and /或LB = 低电平, WE = 低电平定义. 信号必须 valid state to initiate a Write, but any can be deasserted to terminate the Write. The to the rising or falling edge of the signal that terminates the Write.

t_{sa}, t_{ha}, t_{sd} 和 t_{hd} 时间 参考

2. 在 WE = LOW to place the I/O in a HIGH-Z state 之前的最小值 4ns 内测试.

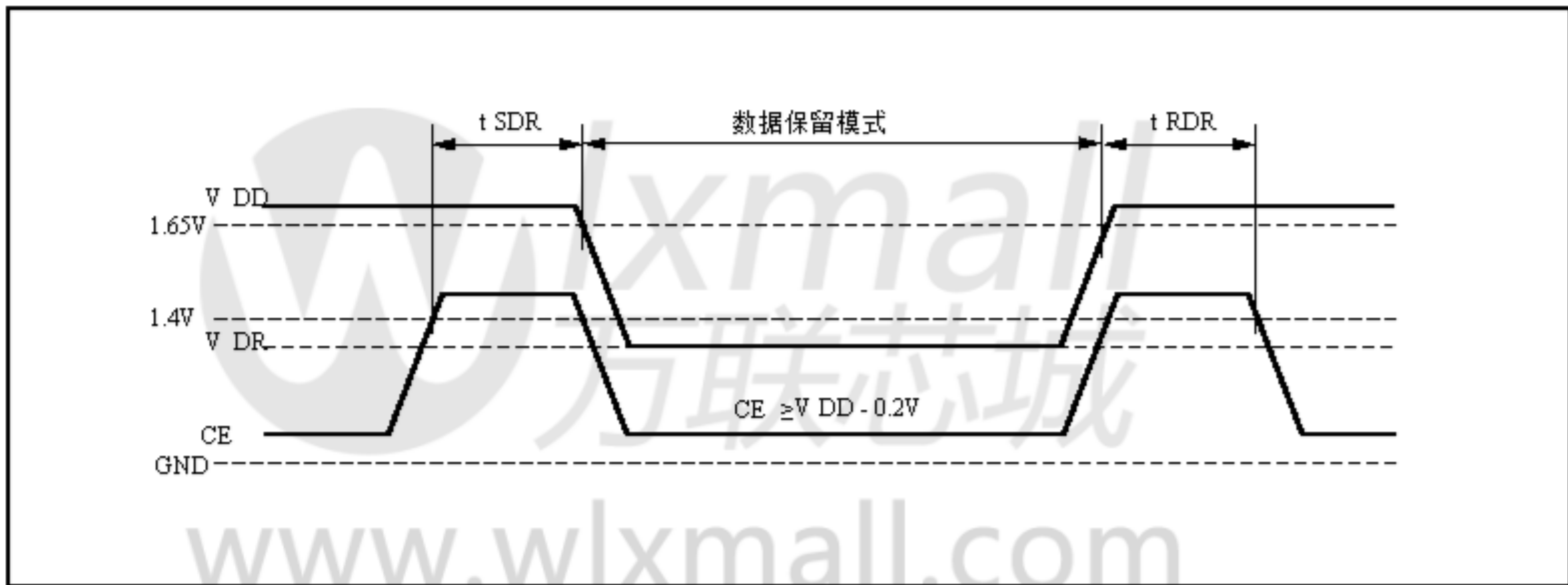
3. WE may be held LOW across many address cycles and the LB, UB pins can be 可以控制写作功能.

数据保持切换特性 (LL)

符号	参数	测试条件	选项	闭.	典型. (1	最大.	单元
V _{博士}	V _{DD for Data Retention}	See Data Retention Waveform		2.0	-	3.6	V
我 _{博士}	Data Retention Current	V _{DD} = 2.0V, $C_E \leq V_{DD} - 0.2V$	COM. 工业.	- -	五 -	10 15	嘛
t _{sDr}	Data Retention Setup Time	See Data Retention Waveform		0	-	-	NS
t _{rDr}	恢复时间	See Data Retention Waveform		t _{rc}	-	-	NS

注1: 典型值测量V_{DD} = 3.0V, T_a = 25 °C, 未经100%测试.

数据保持波形 (CE Controlled)



订购信息

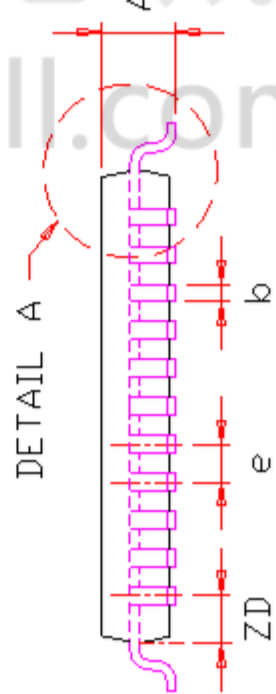
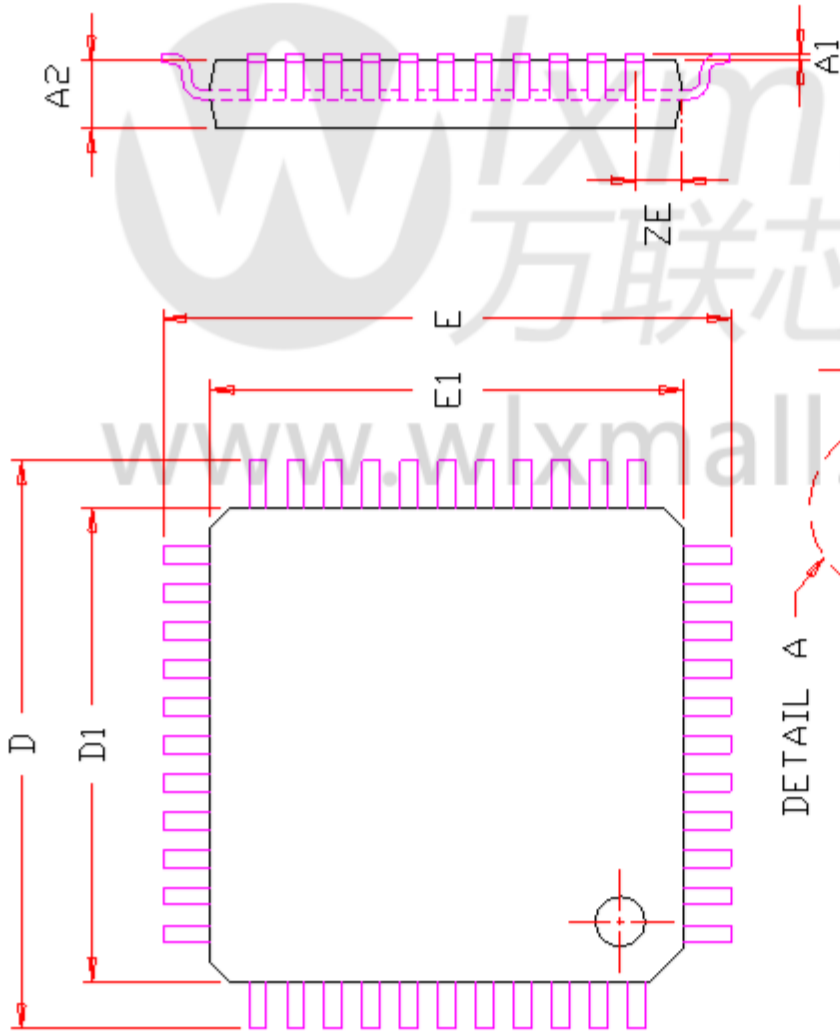
商业范围：0°C至+ 70°C

速度 (ns)	订货号	包
10	IS61LV25616AL-10T	TSOP (II型)
	IS61LV25616AL-10TL	TSOP (II型), 无铅
	IS61LV25616AL-10K	400 milSOJ
12	IS61LV25616AL-12T	TSOP (II型)

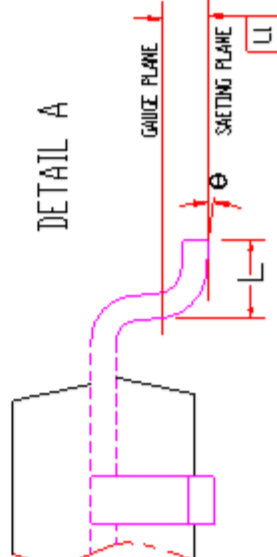
工业范围：-40°C至+ 85°C

速度 (ns)	订货号	包
10	IS61LV25616AL-10TI	TSOP (II型)
	IS61LV25616AL-10TLI	TSOP (II型), 无铅
	IS61LV25616AL-10KI	400 milSOJ
	IS61LV25616AL-10KLI	400 milSOJ, 无铅
	IS61LV25616AL-10LQI	LQFP
	IS61LV25616AL-10LQLI	LQFP, 无铅
	IS61LV25616AL-10BI	MiniBGA (8mmx10mm)
	IS61LV25616AL-10BLI	MiniBGA (8mmx10mm), 无铅
12	IS61LV25616AL-12TI	TSOP (II型)

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.40		1.60	0.055		0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.30		0.45	0.012		0.018
D	11.70	12.00	12.30	0.460	0.472	0.484
D1	9.87	10.00	10.13	0.389	0.394	0.399
E	11.70	12.00	12.30	0.460	0.472	0.484
E1	9.87	10.00	10.13	0.389	0.394	0.399
e	0.80 BSC.			0.031 BSC.		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	0.25 BSC.			0.010 BSC.		
ZD	1.00 REF.			0.039 REF.		
ZE	1.00 REF.			0.039 REF.		
θ	0	3.5°	7°	0	3.5°	7°



DETAIL A



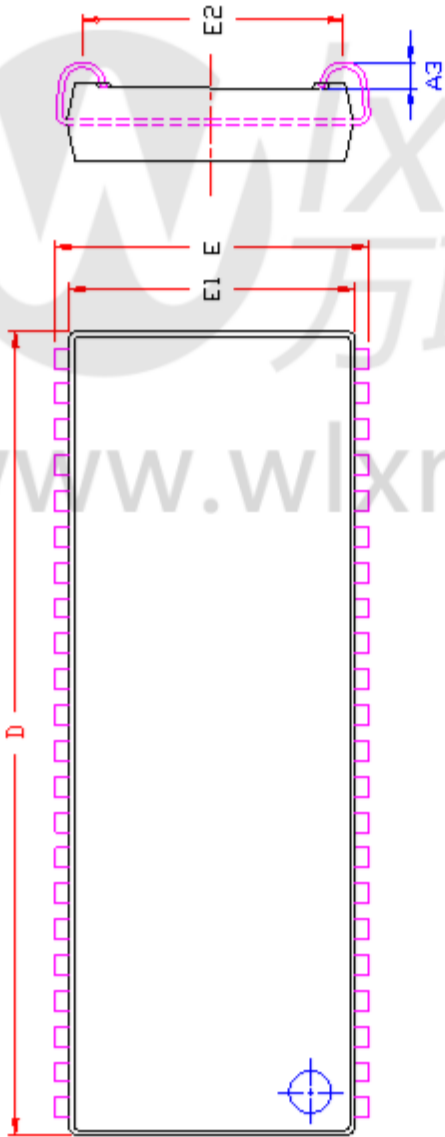
DETAIL A

NOTE:

1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

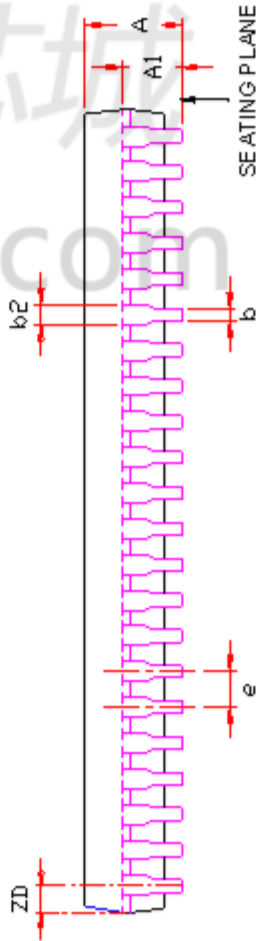
ICSI	TITLE	44L 10x10x1.4mm LQFP (Footprint : 2.0 mm) Package Outline	REV.	C	DATE	08/30/2001
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SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	3.25		3.76	0.128		0.148
A1	2.08			0.082		
A3	0.635			0.025		
b	0.38		0.51	0.015		0.020
b2	0.66	0.71	0.81	0.026	0.028	0.032
D	28.45	28.58	28.70	1.120	1.125	1.130
E	11.05	11.18	11.30	0.435	0.440	0.445
E1	10.03	10.16	10.29	0.395	0.400	0.405
E2		9.40	BSC.		0.370	BSC.
e		1.27	BSC.		0.050	BSC.
ZD		0.95	REF.		0.037	REF.



NOTE :

1. Controlling dimension : mm
2. Dimension D and E1 do not include mold protrusion .
3. Dimension b2 does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.
5. Reference document : JEDEC SPEC MS-027.



TITLE

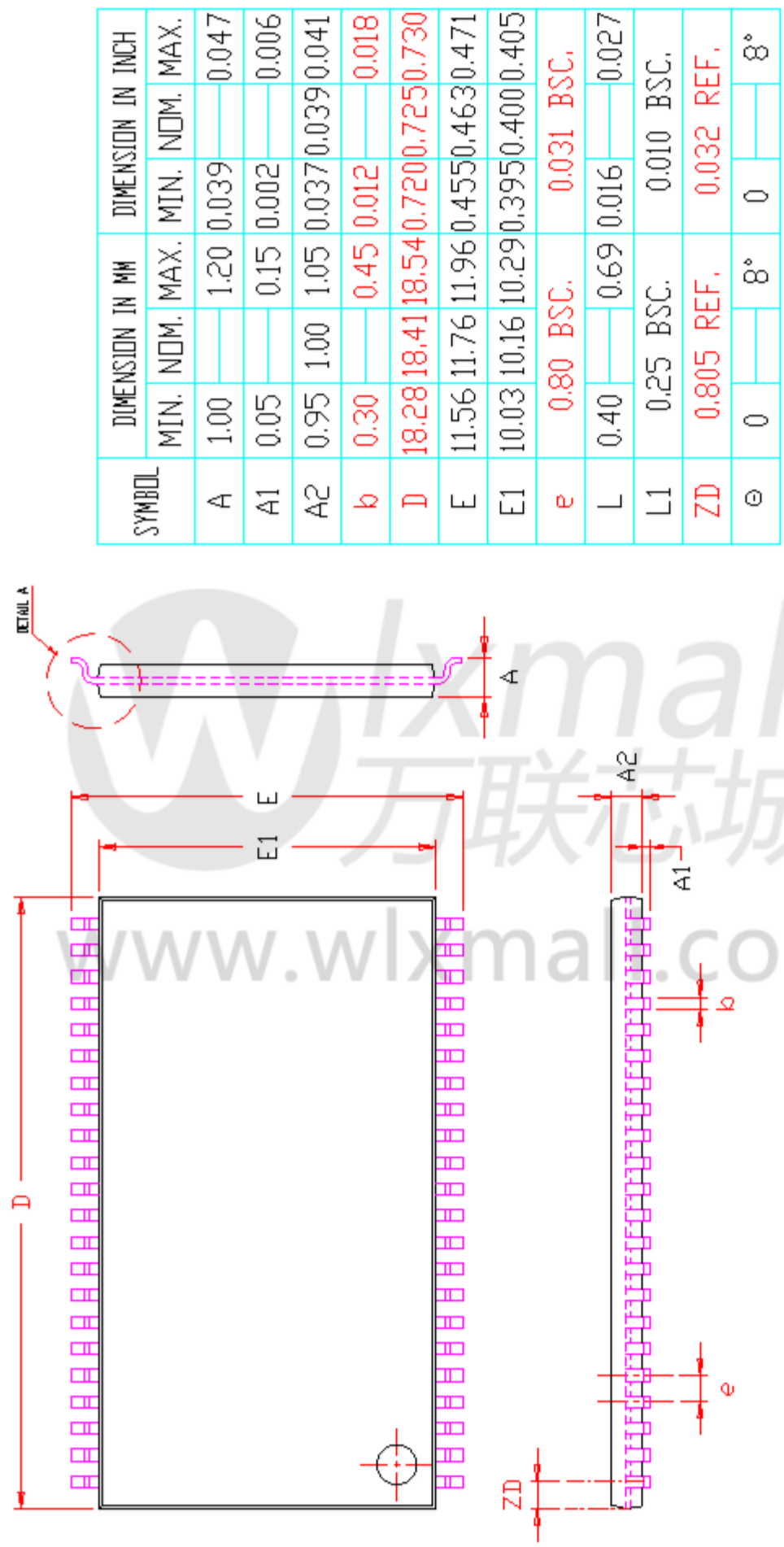
44L 400mil SOJ
Package Outline

REV.

E

DATE

12/21/2007



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00		1.20	0.039		0.047
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30		0.45	0.012		0.018
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	0.80	BSC.		0.031	BSC.	
L	0.40		0.69	0.016		0.027
L1	0.25	BSC.		0.010	BSC.	
ZD	0.805	REF.		0.032	REF.	
⊙	0		8°	0		8°

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION

ISSI	TITLE	44L 400mil TSOP-2 Package Outline	REV.	F	DATE	06/04/2008
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