dsPIC33 DSC Peripheral Integration

Quick Reference Guide

Product Family	Maximum MHz	Program Flash Memory (KB)	RAM (KB)	Pin Count	ADC (resolution)[1]	DAC (resolution)[2]	HS Comp	OPA/PGA	SCCP	MCCP	PWM	MC PWM	SMPS PWM	IC and OC	PWM Resolution (ns)	16-bit/32-bit Timers	QEI	Flash Error Correction Code	RAM MBIST	LVD	WDT	DMT	CRC	Hardware Safety Features[3]	Functional Safety - ISO 26262/ IEC 61508	IEC 60730 Class B Safety	USB	CAN/CAN FD	UART	LIN	I^2C	SPI	I^2S™	SENT	CTMU and mTouch® Sensing	CodeGuard Security - Secure Boot	Flash OTP by ICSP™ Write Inhibit	Embedded Security with ATECC608/TA100	Dual Partition Flash	CLC	PPS	PTG	DMA	DOZE, IDLE, SLEEP and PMD
					Peripheral Function Focus																																							
					Integrated Analog				**Waveform Control**							**Clocks and Timers**		**Safety and Monitoring**									**Communications**								**User Interface**	**Security**			**System Flexibility**					
dsPIC33CH Family - Dual Core (M – Main Core, S – Secondary Core) and dsPIC33CK Family – Single Core																																												
dsPIC33CH128MP5/20x Dual Core	M: 90 S: 100	M: 64–128 S: 24	M: 16 S: 4	28–80	12	12	✓	✓	✓	✓	✓	✓	✓	✓	0.25	✓	✓	✓		✓	✓	✓	✓	L3	✓	✓		✓	✓	✓	✓	✓	✓	✓		✓		✓	✓	✓	✓	✓	✓	✓
dsPIC33CH512MP5/20x Dual Core	M: 90 S: 100	M: 256–512 S: 72	M: 32–48 S: 16	48–80	12	12	✓	✓	✓	✓	✓	✓	✓	✓	0.25	✓	✓	✓	✓	✓	✓	✓	✓	L4	✓	✓		✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓
dsPIC33CK1024MP7xx	100	256-1024	128	48-100	12	12	✓	✓	✓	✓	✓	✓	✓	✓	0.25	✓	✓	✓	✓	✓	✓	✓	✓	L4	✓	✓		✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓
dsPIC33CK512MP6/30x	100	256-512	64	48-80	12	12	✓	✓	✓	✓	✓	✓			0.25	✓	✓	✓	✓	✓	✓	✓	✓	L4	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓
dsPIC33CK256MP5/20x	100	64–256	24	28–80	12	12	✓	✓	✓	✓	✓	✓	✓	✓	0.25	✓	✓	✓	✓	✓	✓	✓	✓	L4	✓	✓		✓	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓
dsPIC33CK64MP10x	100	32–64	8	28–48	12	12	✓	✓	✓	✓	✓	✓	✓	✓	0.25	✓	✓	✓	✓	✓	✓	✓	✓	L4	✓	✓			✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓
dsPIC33CK64MC10x	100	32-64	8	28-48	12	12	✓	✓	✓		✓	✓		✓	2	✓	✓	✓	✓	✓	✓	✓	✓	L4	✓	✓			✓	✓	✓	✓	✓	✓		✓	✓	✓		✓	✓	✓	✓	✓
dsPIC33EV Family																																												
dsPIC33EVXXXGM00X[5V]	70	32–256	4–16	28–64	12	7	✓	✓			✓	✓		✓	7	✓		✓			✓	✓		L3	✓	✓			✓	✓	✓	✓		✓	✓	✓		✓			✓		✓	✓
dsPIC33EVXXXGM10X[5V]	70	32–256	4–16	28–64	12	7	✓	✓			✓	✓		✓	7	✓		✓			✓	✓		L3	✓	✓		✓	✓	✓	✓	✓		✓	✓	✓		✓			✓		✓	✓
dsPIC33EDV Family - Motor Control DSC with Full-Bridge MOSFET Gate Driver																																												
dsPIC33EDV64MC205	70	64	8	52	12	4	✓	✓			✓	✓		✓	7.14	✓	✓				✓		✓	L2		✓			✓	✓	✓	✓			✓						✓	✓	✓	✓
dsPIC33EP Family																																												
dsPIC33EPXXGS2/50X	70	16–64	2–8	28–64	12	12	✓	✓			✓		✓	✓	1	✓					✓			L1	✓	✓			✓		✓	✓	✓						✓		✓			✓
dsPIC33EPXXXGS80X	70	64–128	8	28–80	12	12	✓	✓			✓		✓	✓	1	✓					✓			L1	✓	✓		✓	✓	✓	✓	✓	✓						✓	✓	✓	✓	✓	✓
dsPIC33EPXXGP50X	70	32–512	4–48	28–64	12	4	✓	✓			✓			✓	14	✓					✓		✓	L2		✓		✓	✓	✓	✓	✓			✓						✓	✓	✓	✓
dsPIC33EPXXXMC20X	70	32–256	4–48	28–64	12	4	✓	✓			✓	✓	✓	✓	7	✓	✓				✓		✓	L2		✓			✓	✓	✓	✓			✓						✓	✓	✓	✓
dsPIC33EPXXXMC50X	70	32–512	4–48	28–64	12	4	✓	✓			✓	✓	✓	✓	7	✓	✓				✓		✓	L2		✓		✓	✓	✓	✓	✓			✓						✓	✓	✓	✓
dsPIC33EPXXXGM3XX	70	128–512	16-48	44–100	12	4	✓	✓			✓	✓	✓	✓	7	✓	✓				✓		✓	L2		✓			✓	✓	✓	✓	✓		✓						✓	✓	✓	✓
dsPIC33EPXXXGM6/7XX	70	128–512	16-48	44–100	12	4	✓	✓			✓	✓	✓	✓	7	✓	✓				✓		✓	L2		✓		✓	✓	✓	✓	✓	✓		✓						✓	✓	✓	✓
dsPIC33EPXXXMU8XX	70	256–512	28-52	64–144	12	4	✓				✓	✓	✓	✓	7	✓	✓				✓		✓	L2		✓	✓	✓	✓	✓	✓	✓	✓						✓		✓		✓	✓
dsPIC33EP512GP806	70	512	52	64	12	4	✓				✓			✓	14	✓					✓		✓	L2		✓		✓	✓	✓	✓	✓	✓						✓		✓		✓	✓

1: dsPIC33 DSCs offer SAR ADC and high-speed ADC 2: dsPIC33 DSCs offer general-purpose DAC and audio DAC 3: Hardware Safety Features:
L1: Includes WDT, oscillator fail-safe, illegal opcode detect, TRAP, reset trace, register lock, frequency check, CodeGuard™ security, PWM lock* L2: Includes features of L1 + CRC L3: Includes features of L2 + Flash ECC and/or DMT L4: Includes features of L3 + RAM MBIST
*PWM lock available in devices with MC PWM/SMPS PWM peripheral

(5V) dsPIC33 DSCs with 5V operating Voltage

Note: Similar family of devices with fewer variations are grouped with the same color coding

INTEGRATED ANALOG: Sensor Interfacing and Signal Conditioning	
ADC: Analog-to-Digital Converter	General-purpose ADC with up to 10-/12-bit resolution
HS ADC: High-Speed Analog-to-Digital Converter	High-speed SAR ADC with 12-bit resolution and sampling speed of 10 Msps
DAC: Digital-to-Analog Converter	General-purpose DAC with resolution up 16-bit resolution
ΔΣ DAC: Delta-Sigma Digital-to-Analog Converter	Second-order digital bipolar, two output channel Delta-Sigma DAC with stereo operation support
HS Comp: High-Speed Comparator	General-purpose rail-to-rail comparator with <1 ns response time
OPA/PGA: Operational Amplifier and Programmable Gain Amplifiers	General-purpose op amp and PGAs for internal and external signal source conditioning
WAVEFORM CONTROL: PWM Drive and Waveform Generation	
SCCP: Single Capture/Compare/PWM	Multi-purpose 16-/32-bit input capture, output compare and PWM
MCCP: Multiple Capture/Compare/PWM	Multi-purpose 16-/32-bit input capture, output compare and PWM with up to six outputs and an extended range of output control features
PWM: Pulse Width Modulation	16-bit PWM with up to nine independent time bases
MC PWM: Motor Control Pulse Width Modulation	Motor control 16-bit PWM with multiple synchronized pulse-width modulation, up to six outputs with four duty cycle generators and resolution up to 1 ns
SMPS PWM: Power Supply Pulse Width Modulation	Power supply 16-bit PWM with multiple synchronized pulse-width modulation, up to eight outputs with four independent time bases and resolution up to 1 ns
IC: Input Capture	Input capture with an independent timer base to capture an external event
OC: Output Compare	Output compare with an independent time base to compare value with compare registers and generate a single output pulse, or a train of output pulses on a compare match event
CLOCKS AND TIMERS: Signal Measurement with Timing and Counter Control	
16-/32-bit Timer	General-purpose 16-/32-bit timer/counter with compare capability
QEI: Quadrature Encoder Interface	Quadrature encoder interface to increment encoders for obtaining mechanical position data
SAFETY AND MONITORING: Hardware Monitoring and Fault Detection	
Flash ECC: Error Correction Code	ECC detects the presence of single and double bit errors, and corrects single bit error automatically
RAM MBIST: Memory Built-In Self-Test	RAM MBIST tests for functional correctness of all memory locations
LVD: Low-Voltage Detection	LVD detects drops in system operating voltage using an internal reference voltage for comparison, especially in battery-powered applications
WDT: Watch Dog Timer	System supervisory circuit that generates a reset when software timing anomalies are detected within a configurable critical window
DMT: Dead Man Timer	System supervisory circuit that generates a reset when instruction sequence anomalies are detected within a configurable critical window
CRC: Cyclical Redundancy Check with Memory Scan	Automatically calculates CRC checksum of Program/DataEE memory for NVM integrity and a general-purpose 16-bit CRC for use with memory and communications data
Hardware Safety Features	Hardware Safety features include Flash error correction, RAM MBIST, backup system oscillator, WDT, DMT, CRC scan, etc.
Functional Safety - ISO 26262/IEC 61508	Functional Ready Devices are ideal for automotive and industrial safety applications requiring ISO 26262 (ASIL B/C) and IEC 61508 (SIL 2/3) safety compliance.
IEC 60730 Class B Safety	IEC 60730 Functional Safety Ready Devices offers Class B safety diagnostic libraries for designing household applications

COMMUNICATIONS: General, Industrial, Lighting and Automotive	
USB OTG: Universal Serial Bus	USB 2.0 full-speed (host and device), low-speed (host) and On-The-Go (OTG) support
CAN/CAN FD: Controller Area Network	Industrial- and automotive-centric communication bus
UART: Universal Asynchronous Receiver Transceiver	General-purpose full-duplex, 8-bit or 9-bit data serial communications with optional ISO 7816 Smart Card support
LIN: Local Interconnect Network	1. Industrial- and automotive-centric communication bus 2. Support for LIN when using the EUSART
I^2C: Inter-Integrated Circuit	General purpose 2-wire inter IC serial interface for communicating with other peripherals or microcontroller devices
SPI: Serial Peripheral Interface	General-purpose 4-wire synchronous serial interface for communicating with other peripherals or microcontroller devices
I^2S: Data Converter Interface	3-wire synchronous half duplex serial interface to handle the stereo data
SENT: Single-Edge Nibble Transmission	SENT is an unidirectional, single-wire serial communications protocol designed for point-to-point transmission of signal values
USER INTERFACE: Capacitive Touch Sensing and LCD Control	
CTMU and mTouch Sensing: Microchip Proprietary Capacitive Touch Technology Using Charge Time Measurement Unit	Capacitive sensing for touch buttons, sliders and system measurements and detection (e.g. water level, intrusion detection, etc.) using an analog CTMU that provides accurate differential time measurement between pulse sources and asynchronous pulse generation
EMBEDDED SECURITY: Hardware Integrated Cryptographic Engine	
CodeGuard Security - Secure Boot	Allows devices to configure the boot segment as a read-only section of memory to protect the bootloader from modification via remote digital attacks.
Flash OTP by ICSP™ Write Inhibit	Flash OTP by ICSP™ Write Inhibit enables Flash to be configured as One-Time Programmable (OTP) memory with the ability to write and read protect the Flash memory
SYSTEM FLEXIBILITY: System Peripherals and Interconnects	
Dual Partition Flash	Dual partition Flash operation, allowing the support of robust bootloader systems and fail-safe storage of application code, with options designed to enhance code security
CLC: Configurable Logic Cell	Integrated combinational and sequential logic with custom interconnection and re-routing of digital peripherals
PPS: Peripheral Pin Select	I/O pin remapping of digital peripherals for greater design flexibility and improved EMI board layout
PTG: Peripheral Trigger Generator	User-programmable sequencer, capable of generating complex trigger signal sequences to coordinate the operation of other peripherals
DMA: Direct Memory Access	Direct memory access for transfer of data between the CPU and its peripherals without CPU assistance
DOZE, IDLE, SLEEP and PMD	Low-power saving modes

Learn more about dsPIC33 DSCs at
www.microchip.com/dsPIC33C and www.microchip.com/dsPIC33E

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