NXP Solutions for In-Vehicle Networking

		High-Speed CAN												
		PCA82C250T PCA82C251T	TJA1050T	TJA1051T TJA1051T/3 TJA1051T/E TJA1051TK/3	TJF1051T	TJA1057T TJA1057TK	TJA1040T	TJA1042T TJA1042T/3 TJA1042TK/3	TJA1044T TJA1044TK	TJA1048T TJA1048TK Dual HS-Can	TJA1049T(/3) TJA1049TK(/3)	TJA1041(A)	TJA1043T TJA1043TK	TJA1145T TJA1145TK
Status		Production	Production	Production	Production	Production	Production	Production	Production	Production	Production	Production	Production	Production
Physical-Layer Compliance		ISO 11898-2	ISO 11898-2	ISO 11898-2	ISO 11898-2	ISO 11898-2	ISO 11898-2 ISO 11898-5	ISO 11898-2 ISO 11898-5	ISO 11898-2 ISO 11898-5	ISO 11898-2 ISO 11898-5	ISO 11898-2 ISO 11898-5	ISO 11898-2 ISO 11898-5	ISO 11898-2 ISO 11898-5	ISO 11898-2 ISO 11898-5 ISO 11898-6
Bit Rate	bps	<1 Mbps	40 kbps to 1 Mbps	40 kbps to 1 Mbps	40 kbps to 1 Mbps	40 kbps to 1Mbps	40 kbps to 1 Mbps	40 kbps to 1 Mbps	40kbps to 1Mbps	40 kbps to 1 Mbps	40 kbps to 1 Mbps	40 kbps to 1 Mbps	40 kbps to 1 Mbps	15 kbps to 2 Mbps
Operating Modes		Normal, Standby	Normal, Listen only	Normal, Listen only, (Off mode only in TJA1051T/E)	Normal, Listen only	Normal, Listen only	Normal, Standby	Normal, Standby	Normal, Standby	Normal, Standby	Normal, Standby	Normal, Listen only, Standby, Sleep	Normal, Listen only, Standby, Sleep	Normal, Listen only, Standby & Sleep Partial Networking, Standby & Sleep
Package (Lead Free)		SO8	SO8	SO8, HVSON8	SO8	SO8, HVSON8*	SO8	SO8, HVSON8	SO8, HVSON8*	SO14 HVSON14	SO8, HVSON8*	SO14	SO14, HVSON14	SO14 HVSON 14
V_{CC}	V	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	4.75 to 5.25	4.75 to 5.25	4.5 to 5.5	4.75 to 5.25	4.5 to 5.5	4.75 to 5.25	4.75 to 5.25	4.5 to 5.5	4.5 to 5.5
Standby/Sleep Current	µA	100/-	-/-	-/-	-/-	-/-	10/-	10/-	10/-	17/-	10/-	-/20	-/20	44/40
Bus Robustness	V	-8 to +18 (-36 to +36)	-27 to +40	-58 to +58	-58 to +58	-42 to +42	-27 to +40	-58 to +58	-42 to +42	-58 to +58	-58 to +58	-27 to +40	-58 to +58	-58 to +58
Common-Mode Voltage	V	-7 to +12	-12 to +12	-30 to +30	-12 to +12	-12 to +12	-12 to +12	-30 to +30	-12 to +12	-30 to +30	-12 to +12	-12 to +12	-30 to +30	-12 to +12
ESD														
HBM	kV	±2 (PCA82C250) ±2.5 (PCA82C250)	±4	±8	±8	±6	±6	±8	±6	±6	±8	±6	±8	±8
IEC61000-4-2	kV			±8	±8	±6		±8	±6	±6	±8		±8	±6
MCU Interface Level	V	5	3.3 to 5 (inputs)	3 to 5	3 to 5	3 to 5	3.3 to 5 (inputs)	3 to 5	3.3 to 5 (inputs)	3 to 5	3 to 5	3 to 5	3 to 5	2.85 to 5.5
Temperature Range (Tvj)	°C	-40 to +150	-40 to +150	-40 to +150	-40 to +125	-40 to +150	-40 to +150	-40 to +150	-40 to +150	-40 to +150	-40 to +150	-40 to +150	-40 to +150	-40 to +150
Additional Functionality														
		-C250 suitable for 12 V applications -C251 suitable for 24 V applications	Suitable for 12 V applications	Suitable for 24 V applications	Suitable for 24 V applications	Optimized solution for 12 V applications	Suitable for 12 V applications	Suitable for 24 V applications	Optimized solution for 12 V applications	Suitable for 24 V applications	Suitable for 24 V applications	Suitable for 12 V applications	Suitable for 24 V applications	Suitable for use in 12 and 24 V systems
		Slope control	TxD dominant timeout	TxD dominant timeout	TxD dominant timeout	TxD dominant timeout	TxD dominant timeout	TxD dominant timeout	TxD dominant timeout	TxD dominant timeout	TxD dominant timeout	TxD dominant timeout, Local and bus failure diagnosis	TxD dominant timeout, Local and bus failure diagnosis	CAN offline mode with autonomous bus biasing for failure protection
		Vref pin	Vref pin	Pin-compatible with TJA1050	Qualify for industrial automation. Pin-compatible with TJA1050/1051	Pin-compatible with TJA1050/TJA1051	Split pin	Split pin	Pin-compatible with TJA1040/TJA1042	Two independent HS-CAN (TJA1042/3) transceiver, Pin-compatible with TJA1042/3 but software adjustment requried	Split pin	Split pin	Split pin	Supports ISO 11898-6 compliant CAN partial networking by means of a selective wake-up function
				Improved EMC and ESD robustness	Improved EMC and ESD robustness	Improved EMC for removal of common-mode choke		Improved EMC and ESD robustness	Improved EMC for removal of common-mode choke	Improved EMC and ESD robustness	Improved EMC and ESD robustness		Improved EMC and ESD robustness	Improved EMC and ESD robustness
			Can be directly connected to a 3.3 V µC if the µC has 5 V tolerant inputs	/3 with VIO pin for direct interface to 3 V microcontroller		Can be directly connected to a 3.3 V µC if the µC has 5 V tolerant inputs	Can be directly connected to a 3.3 V µC if the µC has 5 V tolerant inputs	/3 with VIO pin for direct interface to 3 V microcontroller	Can be directly connected to a 3.3 V µC if the µC has 5 V tolerant inputs		Pin-compatible with TJA1040 / TJA1042 /3 version		Pin-compatible with TJA1041(A)	VIO input allows for direct interfacing with 3 and 5 V microcontroller
						Dual-sourced solution via two foundries			Dual-sourced solution via two foundries					
							Remote bus wakeup	Remote bus wakeup	Remote bus wakeup	Remote bus wakeup	Remote bus wakeup	Remote bus wakeup, Local wakeup	Remote bus wakeup, Local wakeup	Remote standard & selective wakeup, Local wakeup
Application Note		AN96116	AN00020	AH1014	AH1014	AH1308	AN10211	AH1014	AH1308	AH1014	AH1021	AN00094	AH1014	under preparation

T/3 and TK/3 with VIO pin; direct interface to microcontrollers with supply voltages from 3 to 5 V
T/E with EN pin

		Isolated CAN	
		TJA1052i/5 TJA1052i/2 TJA1052i/1	TJF1052i/5 TJF1052i/2 TJF1052i/1
Status		Production	Production
Physical-Layer Compliance		ISO 11898-2	ISO 11898-2
Bit Rate		40 kbps to 1 Mbps	40 kbps to 1 Mbps
Operating Modes		Normal, Standby (see application note)	Normal, Standby (see application note)
Package (Lead Free)		SO16WB	SO16WB
VDD1	V	3 to 5.25	3 to 5.25
VDD2	V	4.75 to 5.25	4.75 to 5.25
Standby	mA	5.6 mA @VDD1	5.6 mA @VDD1
Bus Robustness	V	±58	±58
Common-Mode Voltage	V	±25	±25
ESD			
HBM	kV	±8	±8
IEC61000-4-2	kV	±6	±6
Temperature Range (Tvj)	°C	-40 to +150	-40 to +125
Isolated Voltage	kV	TJA1052i/5: 5kV TJA1052i/2: 2.5kV TJA1052i/1: 1kV	TJF1052i/5: 5kV TJF1052i/2: 2.5kV TJF1052i/1: 1kV
Additional Functionality			
		Suitable for 24 V applications	Suitable for 24 V applications
		TxD dominant timeout	TxD dominant timeout
		Improved behavior in networks with long stubs	Improved behavior in networks with long stubs
		Can be directly connected to a 3.3 V µC if the µC has 5 V tolerant inputs	Can be directly connected to a 3.3 V µC if the µC has 5 V tolerant inputs
Application Note		AH1301	AH1301

		FT-CAN	
		TJA1055T/CM	TJA1055T/3CM
Status		Production	Production
Physical-Layer Compliance		ISO 11898-3	ISO 11898-3
Bit Rate		40 kbps to 125 kbps	40 kbps to 125 kbps
Operating Modes		Normal, Standby, Sleep, Power-on standby	Normal, Standby, Sleep, Power-on standby
Package (Lead Free)		SO14	SO14
V_{CC}	V	4.75 to 5.25	4.75 to 5.25
Standby/Sleep Current	µA	100 / 100	100 / 100
Bus Robustness	V	-58 to +58	-58 to +58
Common-Mode Voltage	V	na	na
ESD			
HBM	kV	±8	±8
IEC61000-4-2	kV	±6	±6
MCU Interface Level	V	5	3 to 5
Temperature Range (Tvj)	°C	-40 to +150	-40 to +150
Additional Functionality			
		Suitable for 24 V applications	Suitable for 24 V applications
		TxD dominant timeout	TxD dominant timeout
		Pin-compatible with TJA1054	Pin-compatible with TJA1054
		improved EMC and ESD robustness	improved EMC and ESD robustness
		Remote bus wakeup, Local wakeup	Remote bus wakeup, Local wakeup
Application Note		AH0801	AH0801

		CAN FD			
		TJA1145T/FD TJA1145TK/FD	UJA1168TK/FD UJA1168TK/VX/FD	TJA1044GT	TJA1057GT
Description		HS-CAN transceiver fully supporting CAN FD passive and partial networking	Mini System Basis Chip (SBC) including HS-CAN transceiver with Partial Networking and CAN FD-passive, LDO voltage regulator (5 V/150 mA), WAKE input, optional sensor supply (5 V/30 mA), optional INH output	FD transceiver optimized for higher datarate	FD transceiver optimized for higher datarate
Status		Production	Production	Development	Development
Physical-Layer Compliance		ISO 11898-2 ISO 11898-5 ISO 11898-6	ISO 11898-2 ISO 11898-5 ISO 11898-6	ISO 11898-2 ISO 11898-5	ISO 11898-2
Bit Rate	kbps	15 kbps to 1 Mbps	15 kbps to 1 Mbps	40 kbps to 2 Mbps	40 kbps to 2 Mbps
Modes		Normal, Listen only, Standby & Sleep, Partial Networking, Standby & Sleep	Normal, Listen only, Standby & Sleep, Partial Networking, Standby & Sleep	Normal, Standby	Normal, Listen only
Package		SO14, HVSON 14	HVSON14	SO8	SO8
Supply					
VBAT	V	4.5 to 28	3 to 28 V/40 V LDO operational down to 2 V	Not applicable	Not applicable
V_{cc}	V	4.5 to 5.5	Not required	4.75 to 5.25	4.75 to 5.25
ESD (Bus Pins)					
HBM	kV	±8	±8	±6	±6
IEC61000-4-2	kV	±6	±6	±6	±6
MCU Supply and Interface Level	V	3 to 5	5	3.3 to 5.5 (inputs)	3.3 to 5.5 (inputs)
Temperature Range (Tvj)	°C	-40 to +150	-40 to +150	-40 to +150	-40 to +150
System Feature		Supports ISO 11898-6 compliant CAN partial networking by means of a selective wake-up function	5 V (150 mA) LDO output for supply of microcontroller etc. Max 50 mA needed for internal CAN, leaves 100 mA for microcontroller	Optimized solution for 12 V applications	Optimized solution for 12 V applications
		Remote wake-up capability via standard wake-up pattern	Optional protected 5V (30 mA) sensor supply (UJA1168/VX/FD only)	Dual-sourced solution via two foundries	Dual-sourced solution via two foundries
		CAN Offline mode with autonomous bus biasing for failure protection	Window and timeout watchdog with on-chip oscillator, overtemperature warning, programmable undervoltage reset;	Pin-compatible with TJA1040/TJA1042	Pin-compatible with TJA1050/TJA1051
		Suitable for use in 12 and 24 V systems	CAN Bus Pins short-circuit-proof to 58 V	Improved EMC for removal of common-mode choke	Improved EMC for removal of common-mode choke
		CAN Bus Pins short-circuit-proof to 58 V	SPI microcontroller interface	Can be directly connected to a 3.3 V µC if the µC has 5 V tolerant inputs	Can be directly connected to a 3.3 V µC if the µC has 5 V tolerant inputs
		VIO input allows for direct interfacing with 3 to 5 V microcontrollers	Overtemperature shutdown	Maximum loop delay of 210 ns allowing longer cables	Maximum loop delay of 210 ns allowing longer cables
		No wakeups due to CAN FD frame detection		Loop delay symmetry +5% / -15%	Loop delay symmetry +5% / -15%
		Local wakeup		TxD dominant timeout	TxD dominant timeout

		CAN Controller
		SJA1000
Description		Standalone CAN controller support CAN 2.0B
Status		Production
Bit Rate	bps	≤1Mbps
Vdd	V	4.5 to 5.5
Idd	mA	15
Ism (Sleep-Mode Supply Current)	µA	40
Package		DIP28, SO28
ESD	kV	±1.5 kV HBM
Tamb	°C	-40 to +125
System Feature		Extended receive buffer, 64-byte FIFO
		24 MHz clock frequency
		Programmable CAN output driver configuration
PeliCAN Mode with New Feature		Error counters with read/write access
		Programmable error warning limit
		Last error code register
		Error interrupt for each CAN-bus error
		Arbitration lost interrupt with detailed bit position
		Single-shot transmission (no retransmission)
		Listen only mode (no acknowledge, no active error flags)
		Hot plugging support (software-driven bit rate detection)
		Accepttance filter extension (4-byte code, 4-byte mask)
		Self-reception request (receives own messages)

		LIN				
		TJA1020	TJA1021	TJA1027	TJA1029	TJA1022
Description		Standalone LIN transceiver	Standalone LIN transceiver	Standalone LIN transceiver	Standalone LIN transceiver	Dual LIN transceiver
Status		Production	Production	Production	Production	Production
Physical-Layer Compliance		LIN 1.3	LIN 2.x/ SAE J2602	LIN 2.x/ SAE J2602	LIN 2.x/ SAE J2602	LIN 2.x/ SAE J2602
Bit Rate	kBd	2.4 to 20	1 to 20	0 to 20	2.4 to 20	2.4 to 20
Operating Mode		Normal slope, Low slope, Standby, Sleep	Normal, Power-on, Standby, Sleep	Normal, Standby, Sleep	Normal, Standby, Sleep	Normal, Standby, Sleep
Package (Lead Free)		SO8	SO8, HVSON8	SO8, HVSON8	SO8, HVSON8	SO14, HVSON14
Supply						
VBAT	V	5 to 27	5.5 to 27	5 to 18	5 to 18	5 to 18
V_{CC}	V	Not required				
Sleep Current	µA	3	7	7	7	7
Bus Input Range	V	-27 to +40	-40 to +40	-42 to +42	-42 to +42	-42 to +42
ESD						
HBM	kV	±4	±8	±8	±8	±8
IEC61000-4-2	kV		±6	±8	±8	±8
MCU Interface Level	V	3.0 to 5	3.0 to 5	3.0 to 5	3.0 to 5	3.0 to 5
Temperature Range (Tvj)	°C	-40 to +150	-40 to +150	-40 to +150	-40 to +150	-40 to +150
Additional Functionality						
		K-line compatible	K-line compatible	K-line compatible	K-line compatible	K-line compatible
		Wake-up source recognition	Wake-up source recognition			
		Remote bus wakeup	Remote bus wakeup	Remote bus wakeup	Remote bus wakeup	Remote bus wakeup
		Integrated LIN slave termination	Integrated LIN slave termination	Integrated LIN slave termination	Integrated LIN slave termination	Integrated LIN slave termination
		Low slope mode	Low Slope in separate product version			
		INH output	INH output			
		WAKE input	WAKE input			
		TxD dominant timeout	TxD dominant timeout		TxD dominant timeout	TxD dominant timeout
			LIN operation during cranking pulse	LIN operation during cranking pulse	LIN operation during cranking pulse	LIN operation during cranking pulse
		Pin-compatible with TJA1021	Pin-compatible with TJA1020	Pin-compatible with TJA1029	Pin-compatible with TJA1027	Pin-compatible with TJA1027, TJA1029
				Pin-compatible subset of TJA1020, TJA1021	Pin-compatible subset of TJA1020, TJA1021	Pin-compatible subset of TJA1020, TJA1021
Documentation						
Datasheet		www.nxp.com	www.nxp.com	www.nxp.com	www.nxp.com	www.nxp.com
Application Note		AN00093	On request	On request	On request	On request
Certificates						
Conformance		LIN1.3	LIN2.1/J2602	LIN2.1/J2602	LIN2.2/J2602	LIN2.2/J2602
ESD/EMC Report		On request	On request	On request	On request	On request

		LIN Slave Solutions				
		UJA1023	TJA1028	UJA1018	UJA1079A	UJA1069
Description		System on chip including complete LIN I/O Slave with 8 configurable ports. Configuration can be done via the LIN bus. Bit Rate is automatically adapted. 8-bit ADC and PWM integrated.	LIN Slave System Basis Chip including LIN transceiver and voltage regulator	LIN Slave System Basis Chip including LIN transceiver, voltage regulator, 3 LED drivers and LIN Slave Node Position Detection support via LIN switch	System on chip including LIN transceiver, Voltage regulator for microcontroller, Watchdog	Fail-safe System Basis Chip including LIN transceiver, LDO voltage regulator for microcontroller (5V/120 mA), watchdog, WAKE input, High-side switch output with pulse timer, LIMP and EN outputs
Status		Production	Production	Production	Production	Production
Physical-Layer Compliance		LIN 2.0/SAE J2602	LIN 2.x/SAE J2602	LIN 2.x/SAE J2602	LIN 2.x/SAE J2602	LIN 2.x/SAE J2602
Bit Rate	kBd	1 to 20	2.4 to 20	2.4 to 20	1 to 20	2.4 to 20
Modes		Normal, Standby, Sleep, Limp home	Normal, Standby, Sleep	Normal, Standby, Sleep	Normal, Standby, Sleep	Normal, Standby, Sleep, Fail-safe mode
Package		SO16	SO8, HVSON8	HVSON16	HTSSOP32	HTSSOP24/HTSSOP32
Supply						
Vbat	V	5.5 to 27	5.5 to 28	5.5 to 18	4.5 to 28	5.5 to 27 V
Vcc	V	not required				
Standby/Sleep Current	µA	-/45	45/12	47/14	68/49	105/52
Bus Input Range	V	-27 to +40	-40 to +40	-40 to +40	-58 to +58	-60 to +60
ESD (Bus Pins)						
HBM	kV	±8	±8	±8	±8	±8
IEC61000-4-2	kV		±8	±8	±6	±4
MCU Supply	V		3.3/5.0	5.0	3.3/5.0	5.0
System Features		Automatic Bit Rate detection	Voltage regulator with ±2% accuracy and 70 mA capability	Voltage regulator with ±2% accuracy and up to 70 mA capability	Scalable voltage regulator with ±2% accuracy and up to 250 mA capability	5 V LDO output for supply of microcontroller etc.
			Voltage regulator stable with ceramic, tantalum, and aluminum electrolyte capacitors	Voltage regulator stable with ceramic, tantalum, and aluminum electrolyte capacitors	Voltage regulator stable with ceramic, tantalum, and aluminum electrolyte capacitors	
		Configurable sleep mode	Undervoltage reset output	Undervoltage reset output	Programmable undervoltage reset	Programmable undervoltage reset
		Outputs to drive LEDs and PowerFETs	Low-slope version for 10.4 kBd LIN systems	Supports LIN switch method for detection of slave node	Window and timeout watchdog	Enhanced window watchdog with on-chip oscillator. Fully integrated autonomous fail-safe system
		Inputs to read up to 16 switches	Small HVSON8 package option	Small HVSON16 package		HTSSOP32 or HTSSOP24 package
		8 bit AD converter to read		3 high-side outputs to V_{CC}	Global Enable signal to enable safety critical hardware	Global Enable signal to enable safety critical hardware
		8 WAKE inputs			2 WAKE inputs	Local wake-up input. 60 mA High-side output with pulse timer
		Integrated LIN slave termination	Integrated LIN slave termination	Integrated LIN slave termination		
			TxD dominant timeout	TxD dominant timeout	TxD dominant timeout	TxD dominant timeout
			Remote bus wakeup	Remote bus wakeup	Remote bus wakeup	Remote bus wakeup
			LIN operation during cranking pulse	LIN operation during cranking pulse	LIN operation during cranking pulse	
				Pin-compatible subset of TJA1028		
			Pin-compatible subset of UJA1018		Pin-compatible subset of UJA1075, UJA1076, UJA1078	Pin-compatible subset of UJA1061, UJA1065, UJA1066
		Limp home			Limp home	Limp home with LIMP/ INH output
Documentation						
Datasheet		www.nxp.com	www.nxp.com	www.nxp.com	www.nxp.com	www.nxp.com
Application Note		On request	On request	On request	On request	On request
Certificates						
Conformance		LIN2.0/J2602	LIN2.1/J2602	LIN2.2/J2602	LIN2.1/J2602	LIN2.0/J2602
ESD/EMC Report		On request	On request	On request	On request	On request

		FlexRay						
		TJA1080A	TJA1081	TJA1082	TJA1081B	TJA1083	TJA1085	TJA1086
Status		Production	Production	Production	Production	Production	Production	Production
Physical-Layer Compliance		FlexRay V2.1 Rev. A	FlexRay V2.1 Rev. A	FlexRay V2.1 Rev. B	FlexRay V3.0.1 & JASPAR	FlexRay V3.0.1 & JASPAR	FlexRay V3.0.1 & JASPAR	FlexRay V3.0.1 & JASPAR
Bit Rate	kbaud	10000	10000	10000	10000	10000	10000	10000
Operating Modes		Normal, Standby, Receive only, Sleep	Normal, Standby, Receive only, Sleep	Normal, Standby	Normal, Standby, Receive only, Sleep	Normal, Standby	Normal, Standby, Sleep, Reset	Normal, Standby, Sleep, Reset
Package (Lead Free)		SSOP20	SSOP16	TSSOP14	SSOP16	TSSOP14	HVQFN44 (wettable)	HVQFN44 (wettable)
Supply								
VBAT	V	6.5 to 60	6.5 to 60		4.75 to 60		4.75 to 60	4.75 to 60
V_{cc}	V	4.75 to 5.25	4.75 to 5.25	4.75 to 5.25	4.75 to 5.25	4.75 to 5.25	4.75 to 5.25	4.75 to 5.25
Standby/Sleep Current	µA	55	55	30	55	30	55	55
Bus Input Range	V	-60 to +60	-60 to +60	-60 to +60	-60 to +60	-60 to +60	-60 to +60	-60 to +60
ESD								
HBM	kV	±8	±8	±8	±6	±8	±8	±8
IEC61000-4-2	kV			±8	±6	±6	±6	±6
MCU Interface Level	V	2.2 to 5.25	2.2 to 5.25	2.8 to 5.25	2.8 to 5.25	2.8 to 5.25	2.8 to 5.25	2.8 to 5.25
Temperature Range (Tvj)	°C	-40 to +150	-40 to +150	-40 to +150	-40 to +150	-40 to +150	-40 to +150	-40 to +150
Additional Functionality								
		Configurable as bus driver device or active star	Dedicated bus driver device	Dedicated bus driver device	Dedicated bus driver device	Dedicated bus driver device	4-branch active star coupler	2-branch active star coupler
		Supports 60 ns minimum bit time	Supports of 60 ns minimum bit time	Supports of 60 ns minimum bit time	Supports of 60 ns minimum bit time	Supports of 60 ns minimum bit time	Supports of 60 ns minimum bit time	Supports of 60 ns minimum bit time
		Busguardian interface	Busguardian interface	Busguardian interface including feedback	Busguardian interface including feedback	Busguardian interface including feedback	Busguardian interface including feedback	Busguardian interface including feedback
		Remote wake-up via wake-up symbol	Remote wake-up via wake-up symbol	Remote wake-up via wake-up symbol or dedicated FlexRay data frames	Remote wake-up via wake-up symbol or dedicated FlexRay data frames	Remote wake-up via wake-up symbol or dedicated FlexRay data frames	Remote wake-up via wake-up symbol or dedicated FlexRay data frames	Remote wake-up via wake-up symbol or dedicated FlexRay data frames
		Local wake-up	Local wake-up		Local wake-up		Local wake-up	Local wake-up
		ERRN pin	ERRN pin	ERRN pin and SPI	ERRN pin	ERRN pin and SPI	SPI	SPI
Certificates								
Conformance		FlexRay V2.1 Rev. A	FlexRay V2.1 Rev. A	FlexRay V2.1 Rev. B	FlexRay V3.0.1 & JASPAR	FlexRay V3.0.1 & JASPAR	FlexRay V3.0.1 & JASPAR	FlexRay V3.0.1 & JASPAR
Material								
Datasheet		www.nxp.com	www.nxp.com	www.nxp.com	www.nxp.com	www.nxp.com	www.nxp.com	www.nxp.com
Application Note		On request	On request	On request	On request	On request	On request	On request
ESD/EMC Report		On request	On request	On request	On request	On request	On request	On request

		System Basis Chips (SBCs) and Self-Supplied Transceivers						
		UJA1131/32/35/36	UJA1161/62	UJA1163/64/67	UJA1168	UJA1075A/76A/78A	UJA1061	UJA1065/66
Description		System Basis Chip with integrated buck and boost converter (SMPS), LDO voltage regulators for microcontroller (3.3 or 5 V/500 mA) and sensor supply (5 V/100 mA), HS-CAN transceiver, 1x/2x LIN, 2-channel A/D converter, watchdog, 8 general purpose high-voltage IO with PWM, LIMP, and EN outputs	'Self-supplied' HS-CAN transceiver, with HS-CAN transceiver and an internal 5 V CAN supply, optional Sleep mode with INH output and WAKE input	Mini System Basis Chip (SBC) including HS-CAN transceiver, LDO voltage regulator (5 V/150 mA), optional WAKE input, optional sensor supply (5 V/30 mA), optional INH output	Mini System Basis Chip (SBC) including HS-CAN transceiver with Partial Networking, LDO voltage regulator (5 V/150 mA), WAKE input, optional sensor supply (5 V/30 mA), optional INH output	System Basis Chip including HS-CAN transceiver, 0x/1x/2x LIN, LDO voltage regulators for microcontroller (3.3 or 5 V/250 mA) & CAN (5 V/100 mA), optional watchdog, 2 WAKE inputs, WBIAS output with pulse timer, LIMP and EN outputs	Fail-safe System Basis Chip including FT-CAN transceiver, LIN transceiver, LDO voltage regulators for microcontroller (3.3 or 5 V/120 mA) & CAN (5 V/120 mA), watchdog, WAKE input, High-side switch output with pulse timer, LIMP and EN outputs	Fail-safe System Basis Chip including HS-CAN transceiver, 0x/1x LIN transceiver, LDO voltage regulators for microcontroller (3.3 or 5 V/120 mA) & CAN (5 V/120 mA), watchdog, WAKE input, High-side switch output with pulse timer, LIMP and EN outputs
Status		Under development	Production	Production	Production	production	production	production
Physical-Layer Compliance		ISO 11898-2 / ISO 11898-5 Autonomous CAN bus biasing according to ISO 11898-6			ISO 11898-2 / ISO 11898-5 / ISO 11898-6	ISO 11898-2 / ISO 11898-5	ISO11898-3/LIN 2.x/SAE J2602	ISO11898-2/ ISO 11898-5/LIN 2.x/ SAE J2602
Bit Rate	bps	15 kbps to 1Mbps	15 kbps to 1Mbps	15 kbps to 1Mbps	15 kbps to 1Mbps	15 kbps to 1Mbps	<125 kbps	18 kbps to 1Mbps
Modes		Normal, Standby, Sleep	Normal, Standby, Sleep (UJA1162 only)	Normal, Standby, Sleep (UJA1167 only)	Normal, Standby & Sleep, Partial Network, Standby & Sleep	Normal, Standby, Sleep	Normal, standby, sleep, fail-safe	Normal, standby, sleep fail-safe mode
Package		HTQFP48	HVSON14	HVSON14	HVSON14	HTSSOP32	HTSSOP32	HTSSOP32
Supply								
VBAT	V	4 to 28 V/40 V SBC operational down to 2 V	3 to 28 V/40 V	3 to 28 V/40 V LDO operational down to 2V		4.5 to 28 V/40 V	5.5 to 27 V/45 V	5.5 to 27 V/45 V
V_{cc}	V	Not required						
ESD (Bus Pins)								
HBM	kV	±8	±8	±8	±8	±8	±8	±8
IEC61000-4-2	kV	±6	±6	±6	±6	±6	±6	±4
MCU Supply and Interface Level	V	3.3 or 5	2.85 or 5.5	5		3.3 or 5	3.3 or 5	3.3 or 5
Temperature Range (Tvj)	°C	-40 to +150	-40 to +150	-40 to +150	-40 to +150	-40 to +150	-40 to +150	-40 to +150
System Features		Automatic buck&boost DC/DC pre-regulator (SMPS), 5 or 3.3 V (500 mA) LDO output for supply of microcontroller etc.	Internal 5 V LDO for supply of the high-speed CAN transceiver	5 V (150 mA) LDO output for supply of microcontroller etc. Max 50 mA needed for internal CAN, leaves 100 mA for microcontroller		5 or 3.3 V (250 mA) LDO output for supply of microcontroller etc. Optional reduction of internal power dissipation by adding external transistor	5 or 3.3 V LDO output for supply of microcontroller etc.	5 or 3.3 V LDO output for supply of microcontroller etc.
		Auxiliary 5V LDO (100 mA) with optional protection for off-board loads ("sensor supply")		Optional protected 5V (30 mA) sensor supply (UJA1167Vx and UJA1168Vx only)		Auxiliary 5V LDO (100 mA) for supply of the CAN transceiver	Auxiliary 5V LDO (120 mA) for supply of the CAN transceiver	Auxiliary 5V LDO (120 mA) for supply of the CAN transceiver
		Window and timeout watchdog with on-chip oscillator, Limp home, EN output, overtemperature warning & shutdown, programmable undervoltage reset	Overtemperature shutdown, CAN transmitter status signal CTS	All devices: Overtemperature shutdown; UJA1164/67/68: Window and timeout watchdog with on-chip oscillator, overtemperature warning, programmable undervoltage reset; UJA1163: CAN transmitter status signal CTS, undervoltage reset		Optional window and timeout Watchdog, LIMP output, EN output, overtemperature shutdown, programmable undervoltage reset	Enhanced window watchdog with on-chip oscillator. Fully integrated autonomous fail-safe system. LIMP output, EN output, overtemperature warning, programmable undervoltage reset	Enhanced window watchdog with on-chip oscillator. Fully integrated autonomous fail-safe system. LIMP output, EN output, overtemperature warning, programmable undervoltage reset
		CAN Bus Pins short-circuit-proof to ±58 V				CAN & LIN Bus Pins short-circuit-proof to ±58 V	CAN & LIN Bus Pins short-circuit-proof to ±60 V	CAN & LIN Bus Pins short-circuit-proof to ±60 V
		SPI microcontroller interface + 2 interrupt output pins	STBN (UJA1161) or SLPN (UJA1162) input	UJA1164/67/68: SPI microcontroller interface UJA1163: STBN input		SPI microcontroller interface + interrupt output pin	SPI microcontroller interface + interrupt output pin	SPI microcontroller interface + interrupt output pin
		8 protected general purpose high-voltage IO pins with four PWM generators, IOs configurable as high-side driver (HS), low-side driver (LS) or wakeup input	UJA1162: External voltage regulator control (INH pin) and WAKE input	UJA1167/68: WAKE input, Optional INH output Pin (UJA1067 & UJA1068 only)		2 WAKE inputs, WBIAS output with pulse timer	Local wake-up input. 60 mA high-side output with pulse timer	Local wake-up input. 60 mA high-side output with pulse timer
		Two-channel A/D converter with high-voltage inputs for battery monitoring					Partial networking option with global wake-up feature (not ISO11898-6)	Partial networking option with global wake-up feature (not ISO11898-6)

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