



Intel® Agilex™ 7 JTAG Boundary-Scan Testing User Guide



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1. Intel® Agilex™ 7 JTAG BST Overview

Intel® Agilex™ 7 devices support IEEE Std. 1149.1 BST and IEEE Std. 1149.6 BST. When you perform Boundary-Scan Test (BST), you can test pin connections without using physical test probes and capture functional data during normal operation. The boundary-scan cells (BSCs) in a device can force signals onto pins, or capture data from pin or core logic signals. Forced test data is serially shifted into the BSCs. Captured data is serially shifted out and externally compared to expected results.

Intel Agilex 7 devices are implemented using multiple die inside the package, connected together using EMIB (Embedded Multi-die Interconnect Bridge) technology. The multiple die implementation is transparent to BST. There is a single boundary-scan chain for the complete device that includes every die inside the package.

You can perform BST on Intel Agilex 7 devices before, after, and during configuration.

2. Intel Agilex 7 JTAG BST Architecture

2.1. JTAG Circuitry Functional Model

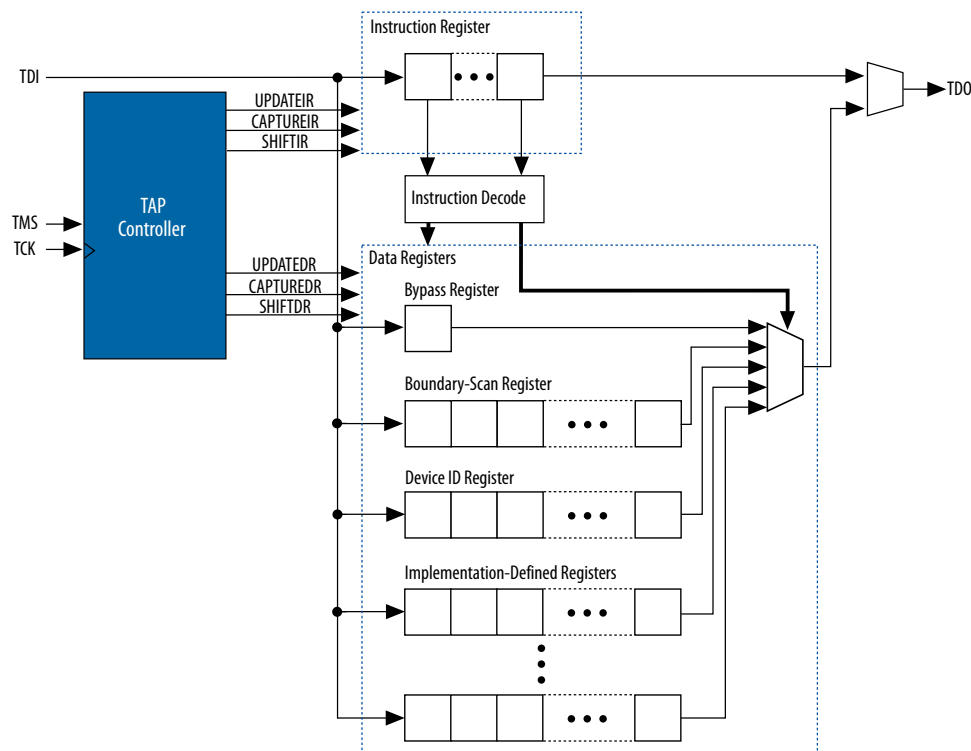
The JTAG BST circuitry requires the following registers:

- Instruction register—determines which action to perform and which data register to access.
- Bypass register (1-bit long data register)—provides a minimum-length serial path between the TDI and TDO pins.
- Boundary-scan register—shift register composed of all the BSCs of the device.

Figure 1. JTAG Circuitry Functional Model

- Test access port (TAP) controller—controls the JTAG BST.
- TMS and TCK pins—operate the TAP controller.
- TDI and TDO pins—provide the serial path for the data and instruction registers.

Note: TRST pin is not available in Intel Agilex 7 devices.



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*Other names and brands may be claimed as the property of others.

2.2. JTAG Pins

Table 1. JTAG Pin Descriptions

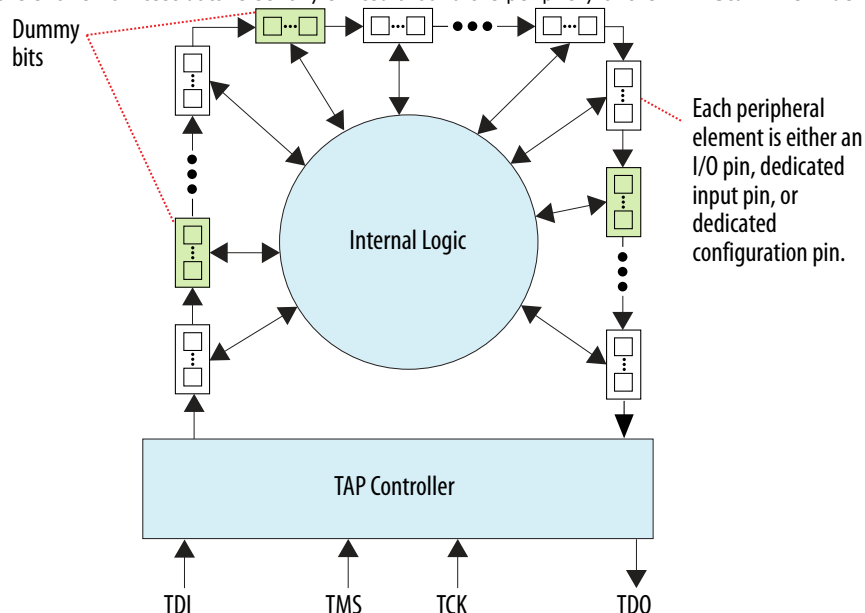
| Pin | Function | Description |
|-----|--|--|
| TDI | Serial input pin for: <ul style="list-style-type: none"> Instructions Test data Programming data | <ul style="list-style-type: none"> TDI is sampled on the rising edge of TCK and should be driven on the falling-edge of TCK. TDI pins have internal weak pull-up resistors. |
| TDO | Serial output pin for: <ul style="list-style-type: none"> Instructions Test data Programming data | <ul style="list-style-type: none"> TDO is driven on the falling edge of TCK and should be sampled on the rising-edge of TCK. The pin is tri-stated if data is not being shifted out of the device. |
| TMS | Input pin that provides the control signal to determine the transitions of the TAP controller state machine. | <ul style="list-style-type: none"> TMS is sampled on the rising edge of TCK and should be driven on the falling-edge of TCK. TMS pins have internal weak pull-up resistors. |
| TCK | The clock input to the BST circuitry. | — |

2.3. IEEE Std. 1149.1 Boundary-Scan Register

The boundary-scan register is a large serial shift register that uses the TDI pin as an input and the TDO pin as an output. The boundary-scan register consists of boundary-scan cells for each I/O pin and padding bits. You can use the boundary-scan register to test external pin connections or to capture internal data.

Figure 2. Boundary-Scan Register

This figure shows how test data is serially shifted around the periphery of the IEEE Std. 1149.1 device.



Note: Dummy bits are present in the scan-chain and must be ignored when read and must be written with 0.

The data signal path for the boundary-scan register runs from the serial data in (SDI) signal to the serial data out (SDO) signal. The scan register begins at the TDI pin and ends at the TDO pin of the device.

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Table 2. Boundary-Scan Cell Descriptions for Intel Agilex 7 Devices

This table lists the capture and update register capabilities of all BSCs within Intel Agilex 7 devices.

| Pin Type | Captures | | | Drives | | | Comments |
|--|-------------------------|---------------------|------------------------|------------------------|--------------------|-----------------------|----------------------------------|
| | Output Capture Register | OE Capture Register | Input Capture Register | Output Update Register | OE Update Register | Input Update Register | |
| User I/O pins | OUTJ | OEJ | PIN_IN | PIN_OUT | PIN_OE | INJ | — |
| Dedicated input | 0 | 1 | PIN_IN | N.C. | N.C. | N.C. | PIN_IN drives to the core logic |
| Dedicated bidirectional ⁽¹⁾ | 0 | OEJ | PIN_IN | N.C. | N.C. | N.C. | PIN_IN drives to the core logic |
| Dedicated output ⁽²⁾ | OUTJ | 0 | 0 | N.C. | N.C. | N.C. | OUTJ drives to the output buffer |

2.4. IEEE Std. 1149.6 Boundary-Scan Register

The BSCs for high-speed serial interface (HSSI) transmitters (TX[p,n]) and receivers/input clock buffers (RX[p,n])/(REFCLK[p,n]) in Intel Agilex 7 devices are different from the BSCs for the I/O pins.

Note: You have to use the EXTEST_PULSE JTAG instruction for AC-coupling on HSSI transceiver. Do not use the EXTEST JTAG instruction for AC-coupling on HSSI transceiver. You can perform AC JTAG on the Intel Agilex 7 device before, after, and during configuration.

⁽¹⁾ This includes the NCONFIG, MSEL0, MSEL1, and MSEL2 pins.

⁽²⁾ This includes the CONF_DONE and NSTATUS pins.

3. Intel Agilex 7 BST Operation Control

3.1. Device ID

The device ID is unique for each Intel Agilex 7 device. Use this code to identify the devices in a JTAG chain.

Table 3. Device ID Information for Intel Agilex 7 Devices

| Product Line | Device ID (32 bits) | | | |
|---------------|---------------------|-----------------------|--------------------------------|-------------|
| | Version (4 bits) | Part Number (16 Bits) | Manufacture Identity (11 Bits) | LSB (1 Bit) |
| AGFA006R16A | 0001 | 0011 0100 0011 0001 | 000 0110 1110 | 1 |
| AGFA008R16A | 0000 | 0011 0100 0011 0001 | 000 0110 1110 | 1 |
| AGFA008R24C | 0010 | 0011 0100 0011 0001 | 0000 1101 110 | 1 |
| AGFA012R24A | 0101 | 0011 0100 0001 0010 | 000 0110 1110 | 1 |
| AGFA012R24B | 1101 | 0011 0100 0001 0010 | 000 0110 1110 | 1 |
| AGFA014R24AR0 | 0000 | 0011 0100 0001 0010 | 000 0110 1110 | 1 |
| AGFA014R24A | 0100 | 0011 0100 0001 0010 | 000 0110 1110 | 1 |
| AGFA014R24B | 1100 | 0011 0100 0001 0010 | 000 0110 1110 | 1 |
| AGFA014R24C | 1100 | 0011 0100 0011 0010 | 0000 1101 110 | 1 |
| AGFA019R25A | 0001 | 0011 0100 0001 0101 | 000 0110 1110 | 1 |
| AGFA022R24C | 0001 | 0011 0100 0011 0011 | 000 0110 1110 | 1 |
| AGFA022R25A | 0001 | 0011 0100 0001 0011 | 000 0110 1110 | 1 |
| AGFA022R31C | 0001 | 0011 0100 0011 0011 | 0000 1101 110 | 1 |
| AGFA023R25AR0 | 0000 | 0011 0100 0001 0101 | 000 0110 1110 | 1 |
| AGFA023R25A | 0000 | 0011 0100 0001 0101 | 000 0110 1110 | 1 |
| AGFA027R24CR0 | 0000 | 0011 0100 0011 0011 | 000 0110 1110 | 1 |
| AGFA027R24CR2 | 0000 | 0011 0100 0011 0011 | 000 0110 1110 | 1 |
| AGFA027R24C | 0000 | 0011 0100 0011 0011 | 000 0110 1110 | 1 |
| AGFA027R25AR0 | 0000 | 0011 0100 0001 0011 | 000 0110 1110 | 1 |
| AGFA027R25A | 0000 | 0011 0100 0001 0011 | 000 0110 1110 | 1 |
| AGFA027R31C | 0000 | 0011 0100 0011 0011 | 000 0110 1110 | 1 |
| AGFB006R16A | 0001 | 0011 0100 0011 1001 | 000 0110 1110 | 1 |
| AGFB008R16A | 0000 | 0011 0100 0011 1001 | 000 0110 1110 | 1 |

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| Product Line | Device ID (32 bits) | | | |
|---------------|---------------------|-----------------------|--------------------------------|-------------|
| | Version (4 bits) | Part Number (16 Bits) | Manufacture Identity (11 Bits) | LSB (1 Bit) |
| AGFB008R24C | 0010 | 0011 0100 0011 1001 | 0000 1101 110 | 1 |
| AGFB012R24A | 0101 | 0011 0100 0001 1010 | 000 0110 1110 | 1 |
| AGFB012R24B | 1101 | 0011 0100 0001 1010 | 000 0110 1110 | 1 |
| AGFB014R24AR0 | 0000 | 0011 0100 0001 1010 | 000 0110 1110 | 1 |
| AGFB014R24A | 0100 | 0011 0100 0001 1010 | 000 0110 1110 | 1 |
| AGFB014R24B | 1100 | 0011 0100 0001 1010 | 000 0110 1110 | 1 |
| AGFB014R24C | 1100 | 0011 0100 0011 1010 | 0000 1101 110 | 1 |
| AGFB019R25A | 0001 | 0011 0100 0001 1101 | 000 0110 1110 | 1 |
| AGFB022R24C | 0001 | 0011 0100 0011 1011 | 000 0110 1110 | 1 |
| AGFB022R25A | 0001 | 0011 0100 0001 1011 | 000 0110 1110 | 1 |
| AGFB022R31C | 0001 | 0011 0100 0011 1011 | 0000 1101 110 | 1 |
| AGFB022R31C | 0001 | 0011 0100 0011 1011 | 000 0110 1110 | 1 |
| AGFB023R25AR0 | 0000 | 0011 0100 0001 1101 | 000 0110 1110 | 1 |
| AGFB023R25A | 0000 | 0011 0100 0001 1101 | 000 0110 1110 | 1 |
| AGFB027R24CR0 | 0000 | 0011 0100 0011 1011 | 000 0110 1110 | 1 |
| AGFB027R24CR2 | 0000 | 0011 0100 0011 1011 | 000 0110 1110 | 1 |
| AGFB027R24C | 0000 | 0011 0100 0011 1011 | 000 0110 1110 | 1 |
| AGFB027R25AR0 | 0000 | 0011 0100 0001 1011 | 000 0110 1110 | 1 |
| AGFB027R25A | 0000 | 0011 0100 0001 1011 | 000 0110 1110 | 1 |
| AGFB027R31C | 0000 | 0011 0100 0011 1011 | 000 0110 1110 | 1 |
| AGFC019R25A | 0011 | 0011 0100 0001 0101 | 000 0110 1110 | 1 |
| AGFC023R25AR0 | 0010 | 0011 0100 0001 0101 | 000 0110 1110 | 1 |
| AGFC023R25A | 0010 | 0011 0100 0001 0101 | 000 0110 1110 | 1 |
| AGFD019R25A | 0011 | 0011 0100 0001 1101 | 000 0110 1110 | 1 |
| AGFD023R25AR0 | 0010 | 0011 0100 0001 1101 | 000 0110 1110 | 1 |
| AGFD023R25A | 0010 | 0011 0100 0001 1101 | 000 0110 1110 | 1 |
| AGIA040R39AR0 | 0000 | 0011 0100 0011 0110 | 0000 1101 110 | 1 |
| AGIB022R29A | 0001 | 0011 0100 1011 1011 | 000 0110 1110 | 1 |
| AGIB022R31B | 0001 | 0011 0100 0011 1011 | 000 0110 1110 | 1 |
| AGIB023R18AR0 | 0000 | 0011 0100 1011 1101 | 0000 1101 110 | 1 |
| AGIB027R29AR0 | 0000 | 0011 0100 1011 1011 | 000 0110 1110 | 1 |
| AGIB027R29AR1 | 0000 | 0011 0100 1011 1011 | 000 0110 1110 | 1 |
| AGIB027R29AR3 | 0000 | 0011 0100 1011 1011 | 000 0110 1110 | 1 |

continued...

| Product Line | Device ID (32 bits) | | | |
|---------------|---------------------|-----------------------|--------------------------------|-------------|
| | Version (4 bits) | Part Number (16 Bits) | Manufacture Identity (11 Bits) | LSB (1 Bit) |
| AGIB027R29A | 0000 | 0011 0100 1011 1011 | 000 0110 1110 | 1 |
| AGIB027R31BR0 | 0000 | 0011 0100 0011 1011 | 000 0110 1110 | 1 |
| AGIB027R31B | 0000 | 0011 0100 0011 1011 | 000 0110 1110 | 1 |
| AGIB041R29DR0 | 0000 | 0011 0100 1011 1111 | 0000 1101 110 | 1 |
| AGIB041R29DR1 | 0000 | 0011 0100 1011 1111 | 0000 1101 110 | 1 |
| AGIB041R29D | 0100 | 0011 0100 1011 1111 | 0000 1101 110 | 1 |
| AGIC040R39AR0 | 0000 | 0011 0100 0011 1110 | 0000 1101 110 | 1 |
| AGIC041R29DR0 | 0010 | 0011 0100 1011 0111 | 0000 1101 110 | 1 |
| AGIC041R29DR1 | 0010 | 0011 0100 1011 0111 | 0000 1101 110 | 1 |
| AGIC041R29D | 0110 | 0011 0100 1011 0111 | 0000 1101 110 | 1 |
| AGID023R18AR0 | 0010 | 0011 0100 1011 1101 | 0000 1101 110 | 1 |
| AGID041R29DR1 | 0010 | 0011 0100 1011 1111 | 0000 1101 110 | 1 |
| AGID041R29D | 0110 | 0011 0100 1011 1111 | 0000 1101 110 | 1 |

3.2. Supported JTAG Instructions

Table 4. JTAG Instructions Supported by Intel Agilex 7 Devices

Caution: Never invoke instruction codes other than the supported JTAG instructions in the following table. Invoking unsupported instruction can damage and render the device unusable.

| JTAG Instruction | Instruction Code | Description |
|--------------------------------|------------------|---|
| MISCCTRL | 00 0001 0011 | <ul style="list-style-type: none"> Required instruction to enable the boundary-scan circuitry for JTAG BST. Set the LSB of the 8-bit data register to '1' and the remaining bits to '0' to enable the boundary-scan circuitry. |
| SAMPLE ⁽³⁾ /PRELOAD | 00 0000 0101 | <ul style="list-style-type: none"> Allows you to capture and examine a snapshot of signals at the device pins during normal device operation and permits an initial data pattern to be an output at the device pins. Use this instruction to preload the test pattern into the update registers before loading the EXTEST instruction. |
| EXTEST | 00 0000 1111 | <ul style="list-style-type: none"> Board-level interconnects by forcing a test pattern at the output pins, and capturing the test results at the input pins. Forcing known logic high and low levels on output pins allows you to detect opens and shorts at the pins of any device in the scan chain. The high-impedance state of EXTEST is overridden by bus hold and weak pull-up resistor features. |
| BYPASS | 11 1111 1111 | <ul style="list-style-type: none"> Places the 1-bit bypass register between the TDI and TDO pins. During normal device operation, the 1-bit bypass register allows the BST data to pass synchronously through the selected devices to adjacent devices. You will get a '0' reading in the bypass register out. |

continued...

⁽³⁾ SAMPLE instruction is not supported for HSSI pins.

| JTAG Instruction | Instruction Code | Description |
|------------------|------------------|---|
| USERCODE | 00 0000 0111 | <ul style="list-style-type: none"> Selects the 32-bit USERCODE register and places it between the TDI and TDO pins to allow serial shifting of USERCODE out of TDO. The 32-bit USERCODE is a programmable user-defined pattern. <p><i>Note:</i> You can set this programmable user-defined number in the Intel Quartus® Prime Pro Edition software.</p> |
| IDCODE | 00 0000 0110 | <ul style="list-style-type: none"> Identifies the devices in a JTAG chain. When the IDCODE register is selected by the IR then in the CAPTURE_DR state, the IDCODE instruction places the 32-bit Device ID register between the TDI and TDO pins to allow serial shifting of Device ID out of TDO. Selects the Device ID register and places it between the TDI and TDO pins to allow serial shifting of Device ID register out of TDO. IDCODE instruction is the default instruction in the Test-Logic-Reset state. |
| HIGHZ | 00 0000 1011 | <ul style="list-style-type: none"> Sets all user I/O pins to an inactive drive state. Places the 1-bit bypass register between the TDI and TDO pins. If you are testing the device after configuration, the programmable weak pull-up resistor or the bus hold feature overrides the HIGHZ value at the pin. |
| CLAMP | 00 0000 1010 | <ul style="list-style-type: none"> Places the 1-bit bypass register between the TDI and TDO pins. If you are testing the device after configuration, the programmable weak pull-up resistor or the bus hold feature overrides the CLAMP value at the pin. The CLAMP value is the value stored in the update register of the BSC. |
| EXTEST_PULSE | 00 1000 1111 | <p>Enables board-level connectivity checking between the transmitters and receivers that are AC coupled by generating three output transitions:</p> <ul style="list-style-type: none"> Driver drives data on the falling edge of TCK in the UPDATE_IR/DR state. Driver drives inverted data on the falling edge of TCK after entering the RUN_TEST/IDLE state. Driver drives data on the falling edge of TCK after leaving the RUN_TEST/IDLE state. |
| EXTEST_TRAIN | 00 0100 1111 | <p>Behaves the same as the EXTEST_PULSE instruction except that the output continues to toggle on the TCK falling edge provided that the TAP controller is in the RUN_TEST/IDLE state.</p> |

Related Information

[Device ID](#) on page 8

4. Intel Agilex 7 I/O Voltage for JTAG Operation

The Intel Agilex 7 device operating in IEEE Std. 1149.1 and IEEE Std. 1149.6 modes uses four required JTAG pins—TDI, TDO, TMS, and TCK.

The TCK pin has an internal weak pull-down resistor, while the TDI and TMS pins have internal weak pull-up resistors. The V_{CCIO_SDM} supply powers the TDI, TDO, TMS, and TCK pins.

The JTAG pins support 1.8 V LVCMOS I/O standard.

Note: For any voltages higher than 1.8 V, you have to use level shifter. The output voltage of the level shifter for the JTAG pins must be the same as set for the V_{CCIO_SDM} supply.

Table 5. TDO Output Buffer

| TDO Output Buffer Condition | Voltage (V) |
|-----------------------------|-------------|
| V_{CCIO_SDM} | 1.8 |

5. Enabling and Disabling Intel Agilex 7 BST Circuitry

5.1. Enabling BST Circuitry

The IEEE Std. 1149.1 BST circuitry is enabled after the device is configured. If you need to perform the boundary-scan test prior to configuration, you must execute the MISCCTRL instruction upon device power up to enable the BST circuitry.

Example 1. MISCCTRL Instruction for Intel Agilex 7 R-Tiles Devices

```
!Shift 10-bit MISCCTRL instruction (0x013) to Instruction Register
SIR 10 TDI (013);
!Transition to Run-Test-Idle state
STATE IDLE;
!Shift 8-bit data (0x47) to Data Register for BST circuitry enabling
SDR 8 TDI (47);
```

Example 2. MISCCTRL Instruction for All Other Devices

```
!Shift 10-bit MISCCTRL instruction (0x013) to Instruction Register
SIR 10 TDI (013);
!Transition to Run-Test-Idle state
STATE IDLE;
!Shift 8-bit data (0x01) to Data Register for BST circuitry enabling
SDR 8 TDI (01);
```

5.2. Disabling BST Circuitry

To ensure that you do not inadvertently enable the IEEE Std. 1149.1 circuitry when it is not required, disable the circuitry permanently with pin connections as listed in the following table.

Table 6. Pin Connections to Permanently Disable the IEEE Std. 1149.1 Circuitry for Intel Agilex 7 Devices

| JTAG Pins ⁽⁴⁾ | Connection for Disabling |
|--------------------------|--------------------------|
| TMS | V _{CCIO_SDM} |
| TCK | GND |
| TDI | V _{CCIO_SDM} |
| TDO | Leave open |

⁽⁴⁾ The JTAG pins are dedicated. Software option is not available to disable JTAG in Intel Agilex 7 devices.



6. Intel Agilex 7 BST Guidelines

6.1. Performing Intel Agilex 7 Boundary-Scan Testing

You can issue `BYPASS`, `IDCODE`, and `SAMPLE` JTAG instructions before, after, or during configuration without having to interrupt configuration.

To interrupt configuration in order to perform BST, you can either hold `nCONFIG` low or issue the following sequence through JTAG: an IR scan updating with `0x201` (`COMMAND`) followed by two 34 bit DR scans updating with `34'h3_0000_0000` then `35'h1_0000_0005`. Once configuration is interrupted, you can issue other JTAG instructions to perform BST.

If you design a board for JTAG configuration using Intel Agilex 7 devices, consider the connections for the dedicated configuration pins.

Dummy Bits

Dummy bits exist in the boundary-scan register during boundary-scan operations in Intel Agilex 7 devices. However, these dummy bits do not have any impact on the pins. The dummy bits appear on the TDO immediately before the corresponding boundary-scan register segment and have an unknown value X, which can be either a 0 or 1.

SoC Devices

For SoC devices, you can only see the FPGA TAP controller in the JTAG chain upon device power up. The TAP controller for the HPS component only appears in the JTAG chain once the device is configured with a programming file/design containing the HPS component. You need to include the information about the HPS component when generating the test patterns for boundary-scan testing. You can download the boundary-scan description language (BSDL) file for the SoC device from the *Intel Agilex 7 Device BSDL Files* page.

F-Tile Devices

For F-tile devices, if FHT support in F-tile is disabled, the boundary-scan cell for the FHT channel is bypassed. Hence, the total boundary-scan length is reduced.

For F-tile devices, if the F-tile is powered down, the boundary-scan cell for the F-tile is bypassed. Hence, the total boundary-scan length is reduced.

Related Information

- [Basic Boundary-Scan Test Troubleshooting Guideline](#)
- [Intel Agilex 7 Device BSDL Files](#)
- [BSDL Support](#)
Provides the post-configuration BSDL generator for Intel Agilex 7 devices.

6.2. Intel Agilex 7 IEEE Std. 1149.1 BST Guidelines

Consider the following guidelines when you perform BST with IEEE Std. 1149.1 devices:

- If the first two bits shifted out of the instruction register in the `SHIFT_IR` state are not 1 and then 0, the TAP controller did not reach the proper state. To solve this problem, try one of the following procedures:
 - Verify that the TAP controller has reached the `SHIFT_IR` state correctly. To advance the TAP controller to the `SHIFT_IR` state, return to the `TEST-LOGIC-RESET` state and send the 01100 code to the TMS pin.
 - Check the connections to the VCC, GND, JTAG, and dedicated configuration pins on the device.
- Perform a `SAMPLE/PRELOAD` test cycle before the first `EXTEST` test cycle to ensure that known data is present at the device pins when you enter `EXTEST` mode. If the `OEJ` update register contains 0, the data in the `OUTJ` update register is driven out. The state must be known and correct to avoid contention with other devices in the system.
- Do not perform `EXTEST` testing during in-circuit reconfiguration because `EXTEST` is not supported during in-circuit reconfiguration.
- After configuration, you cannot test any pins in a differential pin pair. To perform BST after configuration, edit and redefine the BSC group that correspond to these differential pin pairs as an internal cell.

7. Document Revision History for the Intel Agilex 7 JTAG Boundary-Scan Testing User Guide

| Document Version | Changes |
|------------------|--|
| 2023.02.22 | <ul style="list-style-type: none"> Added AGIB041R29DR0, AGIC041R29D, AGID041R29D, AGID041R29DR1, AGIB041R29D, AGIB041R29DR1, AGIC041R29DR1, and AGIC041R29DR0 in the <i>Device ID Information for Intel Agilex 7 Devices</i> table. Rearranged the devices in the <i>Device ID Information for Intel Agilex 7 Devices</i> table according to their suffixes. Updated product family name to "Intel Agilex 7". Retitled the document from <i>Intel Agilex JTAG Boundary-Scan Testing User Guide</i> to <i>Intel Agilex 7 JTAG Boundary-Scan Testing User Guide</i>. |
| 2022.12.19 | <ul style="list-style-type: none"> Added AGFA008R24C, AGFB008R24C, AGFA014R24C, AGFB014R24C, AGIB023R18AR0, AGID023R18AR0, AGIA040R39AR0, AGIC040R39AR0, AGFA022R31C, and AGFB022R31C in the <i>Device ID Information for Intel Agilex Devices</i> table. Added an example in the <i>Enabling BST Circuitry</i> chapter for Intel Agilex R-Tile devices. |
| 2022.04.21 | Added AGFA027R24CR2, AGFB027R24CR2, and AGIB027R29AR3 in the <i>Device ID Information for Intel Agilex Devices</i> table. |
| 2022.01.14 | <p>Added the following devices in the <i>Device ID Information for Intel Agilex Devices</i> table.</p> <ul style="list-style-type: none"> AGFA006R16A AGFA008R16A AGFA019R25A AGFA023R25AR0 AGFA023R25A AGFB006R16A AGFB008R16A AGFB019R25A AGFB023R25AR0 AGFB023R25A AGFC019R25A AGFC023R25AR0 AGFC023R25A AGFD019R25A AGFD023R25AR0 AGFD023R25A |
| continued... | |

| Document Version | Changes |
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| 2021.09.27 | <ul style="list-style-type: none"> Added the following devices in the <i>Device ID Information for Intel Agilex Devices</i> table. <ul style="list-style-type: none"> — AGFA022R24C — AGFA022R31C — AGFA027R24CR0 — AGFA027R24C — AGFA027R31C — AGFB022R24C — AGFB022R31C — AGFB027R24CR0 — AGFB027R24C — AGFB027R31C — AGIB027R29AR0 — AGIB027R29AR1 — AGIB027R31BR0 Updated the following devices in the <i>Device ID Information for Intel Agilex Devices</i> table. <ul style="list-style-type: none"> — AGFA012R24B — AGFA014R24B — AGFB012R24B — AGFB014R24B Added a note for the <code>USERCODE</code> JTAG instruction in the <i>JTAG Instructions Supported by Intel Agilex Devices</i> table. Added a link to the <i>BSDL Support</i> page in the <i>Performing Intel Agilex Boundary-Scan Testing</i> section. |
| 2021.03.29 | <ul style="list-style-type: none"> Updated the HSSI transmitter and receiver pins in the <i>IEEE Std. 1149.6 Boundary-Scan Register</i> section. Removed the following devices from the <i>Device ID Information for Intel Agilex Devices</i> table: <ul style="list-style-type: none"> — AGFA014R17A — AGFB014R17A Added the following devices in the <i>Device ID Information for Intel Agilex Devices</i> table: <ul style="list-style-type: none"> — AGFA012R24A — AGFA012R24B — AGFA014R24AR0 — AGFA014R24B — AGFA027R25AR0 — AGFB012R24A — AGFB012R24B — AGFB014R24AR0 — AGFB014R24B — AGFB027R25AR0 — AGIB022R31B — AGIB027R31B Updated the following devices in the <i>Device ID Information for Intel Agilex Devices</i> table: <ul style="list-style-type: none"> — AGFA014R24A — AGFB014R24A Removed the following sections: <ul style="list-style-type: none"> — <i>IEEE Std. 1149.6 BST Circuitry for Intel Agilex E-Tile Transceiver</i> — <i>IEEE Std. 1149.6 BST Circuitry for Intel Agilex P-Tile Transceiver</i> |
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| 2020.12.14 | <ul style="list-style-type: none"> Added the following devices in the <i>Device ID Information for Intel Agilex Devices</i> table. <ul style="list-style-type: none"> AGIB022R29A AGIB027R29A Added guidelines for Intel Agilex F-tile devices in the <i>Performing Intel Agilex Boundary-Scan Testing</i> section. |
| 2020.09.28 | <ul style="list-style-type: none"> Added the following devices in the <i>Device ID Information for Intel Agilex Devices</i> table. <ul style="list-style-type: none"> AGFA014R17A AGFA022R25A AGFA027R25A AGFB014R17A AGFB022R25A AGFB027R25A Removed the following devices from the <i>Device ID Information for Intel Agilex Devices</i> table. <ul style="list-style-type: none"> AGFA014R24B AGFB014R24B |
| 2019.07.16 | Initial release. |