

Cost-Optimized Portfolio

Product Tables and Product Selection Guide



SPARTAN.6

SPARTAN.7

ARTIX.7

ARTIX.
UltraSCALE+

ZYNQ.

ZYNQ.
UltraSCALE+

CoolRunner-II

AMD
XILINX

Zynq™ UltraScale+™ MPSoCs

| | Device Name ⁽¹⁾ | ZU1CG/EG | ZU2CG/EG | ZU3CG/EG | ZU3TCG/EG | ZU4CG/EG | ZU5CG/EG | ZU6CG/EG | ZU7CG/EG | ZU9CG/EG | |
|--------------------------------|---------------------------------|--|---|----------|-----------|--------------|--------------------------|--------------------------|----------|------------------------|-------|
| Processing System (PS) | Application | Processor Core | | | | | | | | | |
| | Processor Unit | Dual-core/Quad-core Arm® Cortex®-A53 MPCore™ up to 1.3GHz | | | | | | | | | |
| | Real-Time | Memory w/ECC | | | | | | | | | |
| | Processor Unit | L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB | | | | | | | | | |
| | External | Processor Core | | | | | | | | | |
| | Memory | Dual-core Arm Cortex-R5F MPCore up to 533MHz | | | | | | | | | |
| | Connectivity | Dynamic Memory Interface | L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core | | | | | | | | |
| | | Static Memory Interfaces | x16: DDR4 w/o ECC; x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 w/ ECC | | | | | | | | |
| | Integrated Block Functionality | High-Speed Connectivity | NAND, 2x Quad-SPI | | | | | | | | |
| | | General Connectivity | PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet | | | | | | | | |
| Power Management | | 2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO | | | | | | | | | |
| PS to PL Interface | AMS - System Monitor | Full / Low / PL / Battery Power Domains | | | | | | | | | |
| Programmable Logic (PL) | System Logic Cells (K) | 81 | 103 | 154 | 157 | 192 | 256 | 469 | 504 | 600 | |
| | CLB Flip-Flops (K) | 74 | 94 | 141 | 144 | 176 | 234 | 429 | 461 | 548 | |
| | CLB LUTs (K) | 37 | 47 | 71 | 72 | 88 | 117 | 215 | 230 | 274 | |
| | Memory | Distributed RAM (Mb) | 1.0 | 1.2 | 1.8 | 2.1 | 2.6 | 3.5 | 6.9 | 6.2 | 8.8 |
| | | Total Block RAM (Mb) | 3.8 | 5.3 | 7.6 | 5.1 | 4.5 | 5.1 | 25.1 | 11.0 | 32.1 |
| | | UltraRAM (Mb) | - | - | - | 14.0 | 13.5 | 18.0 | - | 27.0 | - |
| | Clocking | Clock Management Tiles (CMTs) | 3 | 3 | 3 | 1 | 4 | 4 | 4 | 8 | 4 |
| | | DSP Slices | 216 | 240 | 360 | 576 | 728 | 1,248 | 1,973 | 1,728 | 2,520 |
| | Integrated IP | PCI Express® | - | - | - | 1x Gen3x8 | 2x Gen3x8 ⁽²⁾ | 2x Gen3x8 ⁽²⁾ | - | 1x Gen3x16 & 1x Gen3x8 | - |
| | | 150G Interlaken | - | - | - | - | - | - | - | - | - |
| 100G Ethernet MAC/PCS w/RS-FEC | | - | - | - | - | - | - | - | - | - | |
| AMS - System Monitor | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | |
| Transceivers | GTH Transceivers ⁽³⁾ | - | - | - | 8 | 16 | 16 | 24 | 24 | 24 | |
| | GTY Transceivers | - | - | - | - | - | - | - | - | - | |
| Speed Grades | Extended ⁽⁴⁾ | -1 -2 -2L | | | | -1 -2 -2L -3 | | | | | |
| | Industrial | | | | | | -1 -1L -2 | | | | |

Notes:
1. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
2. ZU4 and ZU5 also support 1x Gen3x16 based on available GTH.
3. GTH data rates are package dependent:
a) Maximum 12.5Gb/s in SFVC784 and SFVD784
b) Maximum 16.3Gb/s in all other packages
4. -2LE (Tj = 0°C to 110°C). For more details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.

Important: Verify all data in this document with the device data sheets.

Zynq™ UltraScale+™ MPSoCs

PS I/Os⁽¹⁾, 3.3V High-Density (HD) I/O, 1.8V High-Performance (HP) I/Os

PS-GTR 6Gb/s, GTH 16.3Gb/s, GTY 32.75Gb/s

| Pkg Footprint ^(2,3) | Dimensions (mm) | Ball Pitch (mm) | ZU1 | ZU2 | ZU3 | ZU3T | ZU4 | ZU5 | ZU6 | ZU7 | ZU9 |
|--------------------------------|-----------------|-----------------|--------------------------|-------------------------|-------------------------|------------------------|--------------------------|--------------------------|---------------------------|--------------------------|---------------------------|
| A484 | 19x19 | 0.8 | 170, 24, 58 4, 0, 0 | 170, 24, 58 4, 0, 0 | 170, 24, 58 4, 0, 0 | | | | | | |
| A494 | 9.5x15 | 0.5 | 170, 24, 58 4, 0, 0 | | | | | | | | |
| A530 | 9.5x16 | 0.5 | | 170, 24, 58 4, 0, 0 | 170, 24, 58 4, 0, 0 | | | | | | |
| A625 | 21x21 | 0.8 | 170, 24, 156 4, 0, 0 | 170, 24, 156 4, 0, 0 | 170, 24, 156 4, 0, 0 | | | | | | |
| C784 ⁽⁴⁾ | 23x23 | 0.8 | 214, 24, 156, 4, 0, 0 | 214, 96, 156 4, 0, 0 | 214, 96, 156 4, 0, 0 | 214, 72, 52 4, 4, 0 | 214, 96, 156 4, 4, 0 | 214, 96, 156 4, 4, 0 | | | |
| D784 ⁽⁴⁾ | 23x23 | 0.8 | | | | 214, 72, 52 4, 8, 0 | | | | | |
| B900 | 31x31 | 1.0 | | | | | 214, 48, 156 4, 16, 0 | 214, 48, 156 4, 16, 0 | | 214, 48, 156 4, 16, 0 | |
| C900 | 31x31 | 1.0 | | | | | | | 214, 48, 156 4, 16, 0 | | 214, 48, 156 4, 16, 0 |
| B1156 | 35x35 | 1.0 | | | | | | | 214, 120, 208 4, 24, 0 | | 214, 120, 208 4, 24, 0 |
| C1156 | 35x35 | 1.0 | | | | | | | | 214, 48, 312 4, 20, 0 | |
| B1517 | 40x40 | 1.0 | | | | | | | | | |
| F1517 | 40x40 | 1.0 | | | | | | | | 214, 48, 416 4, 24, 0 | |
| C1760 | 42.5x42.5 | 1.0 | | | | | | | | | |
| D1760 | 42.5x42.5 | 1.0 | | | | | | | | | |
| E1924 | 45x45 | 1.0 | | | | | | | | | |

Notes:

1. PS I/O is a combination of PS MIO and PS DDRIO.
2. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other UltraScale devices with the same sequence.
3. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
4. GTH transceivers in the C784 and D784 packages support data rates up to 12.5Gb/s.

Important: Verify all data in this document with the device data sheets.

Zynq™ 7000 SoC Family

| | | Cost-Optimized Devices | | | | | Mid-Range Devices | | | | |
|--|--|---|------------|-------------|---|------------|-------------------|--|--------------|--------------|--------------|
| Processing System (PS) | Device Name | Z-7007S | Z-7012S | Z-7014S | Z-7010 | Z-7015 | Z-7020 | Z-7030 | Z-7035 | Z-7045 | Z-7100 |
| | Part Number | XC7Z007S | XC7Z012S | XC7Z014S | XC7Z010 | XC7Z015 | XC7Z020 | XC7Z030 | XC7Z035 | XC7Z045 | XC7Z100 |
| | Processor Core | Single-Core Arm® Cortex®A9 MPCore™ Up to 766MHz | | | Dual-Core Arm Cortex-A9 MPCore Up to 866MHz | | | Dual-Core Arm Cortex-A9 MPCore Up to 1GHz ⁽¹⁾ | | | |
| | Processor Extensions | NEON™ SIMD Engine and Single/Double Precision Floating Point Unit per processor | | | | | | | | | |
| | L1 Cache | 32KB Instruction, 32KB Data per processor | | | | | | | | | |
| | L2 Cache | 512KB | | | | | | | | | |
| | On-Chip Memory | 256KB | | | | | | | | | |
| | External Memory Support ⁽²⁾ | DDR3, DDR3L, DDR2, LPDDR2 | | | | | | | | | |
| | External Static Memory Support ⁽²⁾ | 2x Quad-SPI, NAND, NOR | | | | | | | | | |
| | DMA Channels | 8 (4 dedicated to PL) | | | | | | | | | |
| Peripherals | 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO | | | | | | | | | | |
| Peripherals w/ built-in DMA ⁽²⁾ | 2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO | | | | | | | | | | |
| Security ⁽³⁾ | RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot | | | | | | | | | | |
| Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only) | 2x AXI 32b Master, 2x AXI 32b Slave 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts | | | | | | | | | | |
| Programmable Logic (PL) | 7 Series PL Equivalent | Artix™ 7 | Artix 7 | Artix 7 | Artix 7 | Artix 7 | Artix 7 | Kintex™ 7 | Kintex 7 | Kintex 7 | Kintex 7 |
| | Logic Cells | 23K | 55K | 65K | 28K | 74K | 85K | 125K | 275K | 350K | 444K |
| | Look-Up Tables (LUTs) | 14,400 | 34,400 | 40,600 | 17,600 | 46,200 | 53,200 | 78,600 | 171,900 | 218,600 | 277,400 |
| | Flip-Flops | 28,800 | 68,800 | 81,200 | 35,200 | 92,400 | 106,400 | 157,200 | 343,800 | 437,200 | 554,800 |
| | Total Block RAM (# 36Kb Blocks) | 1.8Mb (50) | 2.5Mb (72) | 3.8Mb (107) | 2.1Mb (60) | 3.3Mb (95) | 4.9Mb (140) | 9.3Mb (265) | 17.6Mb (500) | 19.2Mb (545) | 26.5Mb (755) |
| | DSP Slices | 66 | 120 | 170 | 80 | 160 | 220 | 400 | 900 | 900 | 2,020 |
| | PCI Express® | — | Gen2 x4 | — | — | Gen2 x4 | — | Gen2 x4 | Gen2 x8 | Gen2 x8 | Gen2 x8 |
| | Analog Mixed Signal (AMS) / XADC ⁽²⁾ | 2x 12 bit, MSPS ADCs with up to 17 Differential Inputs | | | | | | | | | |
| | Security ⁽³⁾ | AES & SHA 256b Decryption & Authentication for Secure Programmable Logic Config | | | | | | | | | |
| | Speed Grades | Commercial | -1 | | | -1 | | | -1 | | |
| Extended | | -2 | | | -2,-3 | | | -2,-3 | | | -2 |
| Industrial | | -1, -2 | | | -1, -2, -1L | | | -1, -2, -2L | | | -1, -2, -2L |

Notes:

- 1 GHz processor frequency is available only for -3 speed grades for devices in flip-chip packages. Please see the data sheet for more details.
- Z-7007S and Z-7010 in CLG225 have restrictions on PS peripherals, memory interfaces, and I/Os. Please refer to the Technical Reference Manual for more details.
- Security block is shared by the Processing System and the Programmable Logic.

Zynq™ 7000 SoC Family

HR I/O, HP I/O, PS I/O, and Transceivers (GTP or GTX)

| | | | Cost-Optimized Devices | | | | | Mid-Range Devices | | | | |
|-----------------------|--------------------------------|-----------------|--|------------------|------------------|--------------------------------|------------------|--|---------------------|---------------------|---------------------|--------|
| Device Name | | | Z-7007S | Z-7012S | Z-7014S | Z-7010 | Z-7015 | Z-7020 | Z-7030 | Z-7035 | Z-7045 | Z-7100 |
| Package Footprint | Dimensions (mm) ⁽¹⁾ | Ball Pitch (mm) | HR I/O, HP I/O PS I/O ⁽²⁾ , GTP Transceivers | | | | | HR I/O, HP I/O PS I/O ⁽²⁾ , GTX Transceivers | | | | |
| CLG225 | 13x13 | 0.8 | 54, 0 84 ⁽³⁾ , 0 | | | 54, 0 84 ⁽³⁾ , 0 | | | | | | |
| CLG400 | 17x17 | 0.8 | 100, 0 128, 0 | | 125, 0 128, 0 | 100, 0 128, 0 | | 125, 0 128, 0 | | | | |
| CLG484 | 19x19 | 0.8 | | | 200, 0 128, 0 | | | 200, 0 128, 0 | | | | |
| CLG485 ⁽⁴⁾ | 19x19 | 0.8 | | 150, 0 128, 4 | | | 150, 0 128, 4 | | | | | |
| SBG485 ⁽⁴⁾ | 19x19 | 0.8 | | | | | | 50, 100 128, 4 | | | | |
| FBG484 | 23x23 | 1.0 | | | | | | 100, 63 128, 4 | | | | |
| FBG676 ⁽¹⁾ | 27x27 | 1.0 | | | | | | 100, 150 128, 4 | 100, 150 128, 8 | 100, 150 128, 8 | | |
| FFG676 ⁽¹⁾ | 27x27 | 1.0 | | | | | | 100, 150 128, 4 | 100, 150 128, 8 | 100, 150 128, 8 | | |
| FFG900 | 31x31 | 1.0 | | | | | | | 212, 150 128, 16 | 212, 150 128, 16 | 212, 150 128, 16 | |
| FFG1156 | 35x35 | 1.0 | | | | | | | | | 250, 150 128, 16 | |

Notes:

1. Devices in the same package are footprint compatible. FBG676 and FFG676 are also footprint compatible.
2. PS I/O count does not include dedicated DDR calibration pins.
3. PS DDR and PS MIO pin count is limited by package size. See DS190, *Zynq 7000 SoC Overview* for details.
4. CLG485 and SBG485 are pin-to-pin compatible. See product data sheets and user guides for more details. See DS190, *Zynq 7000 SoC Overview* for package details.

Artix™ UltraScale+™ FPGAs

| Device Name | AU7P | AU10P | AU15P | AU20P | AU25P |
|---------------------------------|-----------|--------------------------|--------------------------|----------------|----------------|
| System Logic Cells (K) | 82 | 96 | 170 | 238 | 308 |
| CLB Flip-Flops (K) | 75 | 88 | 156 | 218 | 282 |
| CLB LUTs (K) | 37 | 44 | 78 | 109 | 141 |
| Dist. RAM (Mb) | 1.1 | 1.0 | 2.5 | 3.2 | 4.7 |
| Total Block RAM (Mb) | 3.8 | 3.5 | 5.1 | 7.0 | 10.5 |
| 36K Block RAM Blocks | 108 | 100 | 144 | 200 | 300 |
| UltraRAM (Mb) | – | – | – | – | – |
| Clock Management Tiles (CMTs) | 2 | 3 | 3 | 3 | 4 |
| DSP Slices | 216 | 400 | 576 | 900 | 1,200 |
| PCI Express® | 1x Gen3x4 | 1x Gen4x8 ⁽¹⁾ | 1x Gen4x8 ⁽¹⁾ | 1x Gen3x8 | 1x Gen3x8 |
| AMS - System Monitor | 1 | 1 | 1 | 1 | 1 |
| Max. Single-Ended HD I/Os | 144 | 72 | 72 | 72 | 96 |
| Max. Single-Ended HP I/Os | 104 | 156 | 156 | 156 | 208 |
| GTH Transceivers ⁽²⁾ | 4 | 12 | 12 | – | – |
| GTY Transceivers ⁽²⁾ | – | – | – | 12 | 12 |
| Extended | | | -1 -2 | | |
| Industrial | | | -1 -2 -1L | | |
| Package | Dim. (mm) | Ball Pitch (mm) | HD I/O, HP I/O, GTH, GTY | | |
| UBVA368 | 11.5x9.5 | 0.5 | 24, 104, 8, 0 | 24, 104, 8, 0 | |
| SBVB484 | 19x19 | 0.8 | 48, 156, 12, 0 | 48, 156, 12, 0 | |
| SBVC484 | 19x19 | 0.8 | 144, 104, 4, 0 | | |
| SFVB784 | 23x23 | 0.8 | | 72, 156, 0, 12 | 96, 208, 0, 12 |
| FFVB676 | 27x27 | 1.0 | 72, 156, 12, 0 | 72, 156, 12, 0 | 72, 208, 0, 12 |

Notes:

1. PCIe Gen4 is available in AU10P and AU15P in the FFVB676 package. AU10P and AU15P in other packages support Gen3x8.

2. GTH and GTY data rates are package dependent:

- Maximum 12.5Gb/s in UBVA368, SBVB484, SBVC484, SFVB784

- Maximum 16.3Gb/s in FFVB676.

Artix™ 7 FPGAs

Transceiver Optimization at the Lowest Cost and Highest DSP Bandwidth
(1.0V, 0.95V, 0.9V)

| | Part Number | XC7A12T | XC7A15T | XC7A25T | XC7A35T | XC7A50T | XC7A75T | XC7A100T | XC7A200T |
|----------------------------|---|-----------------|-----------------|--|-------------|-------------|-------------|-------------|-------------|
| Logic Resources | Logic Cells | 12,800 | 16,640 | 23,360 | 33,280 | 52,160 | 75,520 | 101,440 | 215,360 |
| | Slices | 2,000 | 2,600 | 3,650 | 5,200 | 8,150 | 11,800 | 15,850 | 33,650 |
| | CLB Flip-Flops | 16,000 | 20,800 | 29,200 | 41,600 | 65,200 | 94,400 | 126,800 | 269,200 |
| Memory Resources | Maximum Distributed RAM (Kb) | 171 | 200 | 313 | 400 | 600 | 892 | 1,188 | 2,888 |
| | Block RAM/FIFO w/ ECC (36 Kb each) | 20 | 25 | 45 | 50 | 75 | 105 | 135 | 365 |
| | Total Block RAM (Kb) | 720 | 900 | 1,620 | 1,800 | 2,700 | 3,780 | 4,860 | 13,140 |
| Clock Resources | CMTs (1 MMCM + 1 PLL) | 3 | 5 | 3 | 5 | 5 | 6 | 6 | 10 |
| I/O Resources | Maximum Single-Ended I/O | 150 | 250 | 150 | 250 | 250 | 300 | 300 | 500 |
| | Maximum Differential I/O Pairs | 72 | 120 | 72 | 120 | 120 | 144 | 144 | 240 |
| Embedded Hard IP Resources | DSP Slices | 40 | 45 | 80 | 90 | 120 | 180 | 240 | 740 |
| | PCI® Gen2 ⁽¹⁾ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Analog Mixed Signal (AMS) / XADC | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Configuration AES / HMAC Blocks | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | GTP Transceivers (6.6 Gb/s Max Rate) ⁽²⁾ | 2 | 4 | 4 | 4 | 4 | 8 | 8 | 16 |
| Speed Grades | Commercial Temp (C) | -1, -2 | -1, -2 | -1, -2 | -1, -2 | -1, -2 | -1, -2 | -1, -2 | -1, -2 |
| | Extended Temp (E) | -2L, -3 | -2L, -3 | -2L, -3 | -2L, -3 | -2L, -3 | -2L, -3 | -2L, -3 | -2L, -3 |
| | Industrial Temp (I) | -1, -2, -1L | -1, -2, -1L | -1, -2, -1L | -1, -2, -1L | -1, -2, -1L | -1, -2, -1L | -1, -2, -1L | -1, -2, -1L |
| | Package ^{(3), (4)} | Dimensions (mm) | Ball Pitch (mm) | Available User I/O: 3.3V SelectIO™ HR I/O (GTP Transceivers) | | | | | |
| | CPG236 | 10 x 10 | 0.5 | | 106 (2) | | 106 (2) | | |
| | CPG238 | 10 x 10 | 0.5 | 112 (2) | | 112 (2) | | | |
| | CSG324 | 15 x 15 | 0.8 | | 210 (0) | | 210 (0) | 210 (0) | 210 (0) |
| | CSG325 | 15 x 15 | 0.8 | 150 (2) | 150 (4) | 150 (4) | 150 (4) | | |
| | FTG256 | 17 x 17 | 1.0 | | 170 (0) | | 170 (0) | 170 (0) | 170 (0) |
| | SBG484 | 19 x 19 | 0.8 | | | | | | 285 (4) |
| Footprint Compatible | FGG484 ⁽⁵⁾ | 23 x 23 | 1.0 | | 250 (4) | | 250 (4) | 285 (4) | 285 (4) |
| | FBG484 ⁽⁵⁾ | 23 x 23 | 1.0 | | | | | | 285 (4) |
| Footprint Compatible | FGG676 ⁽⁶⁾ | 27 x 27 | 1.0 | | | | | 300 (8) | 300 (8) |
| | FBG676 ⁽⁶⁾ | 27 x 27 | 1.0 | | | | | | 400 (8) |
| | FFG1156 | 35 x 35 | 1.0 | | | | | | 500 (16) |

Notes:

1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.
2. Represents the maximum number of transceivers available. Note that the majority of devices are available without transceivers. See the Package section of this table for details.
3. Leaded package option available for all packages. See DS180, *7 Series FPGAs Overview* for package details.
4. Device migration is available within the Artix 7 family for like packages but is not supported between other 7 series families.
5. Devices in FGG484 and FBG484 are footprint compatible.
6. Devices in FGG676 and FBG676 are footprint compatible.

Spartan™ 7 FPGAs

| | | | | I/O Optimization at the Lowest Cost and Highest Performance-per-Watt (1.0V, 0.95V) | | | | | |
|----------------------------|------------------------------------|----------------|-----------------|---|-----------|-----------|-----------|-----------|-----------|
| | | Part Number | | XC7S6 | XC7S15 | XC7S25 | XC7S50 | XC7S75 | XC7S100 |
| Logic Resources | Logic Cells | | | 6,000 | 12,800 | 23,360 | 52,160 | 76,800 | 102,400 |
| | Slices | | | 938 | 2,000 | 3,650 | 8,150 | 12,000 | 16,000 |
| | CLB Flip-Flops | | | 7,500 | 16,000 | 29,200 | 65,200 | 96,000 | 128,000 |
| Memory Resources | Max. Distributed RAM (Kb) | | | 70 | 150 | 313 | 600 | 832 | 1,100 |
| | Block RAM/FIFO w/ ECC (36 Kb each) | | | 5 | 10 | 45 | 75 | 90 | 120 |
| | Total Block RAM (Kb) | | | 180 | 360 | 1,620 | 2,700 | 3,240 | 4,320 |
| Clock Resources | Clock Mgmt Tiles (1 MMCM + 1 PLL) | | | 2 | 2 | 3 | 5 | 8 | 8 |
| I/O Resources | Max. Single-Ended I/O Pins | | | 100 | 100 | 150 | 250 | 400 | 400 |
| | Max. Differential I/O Pairs | | | 48 | 48 | 72 | 120 | 192 | 192 |
| Embedded Hard IP Resources | DSP Slices | | | 10 | 20 | 80 | 120 | 140 | 160 |
| | Analog Mixed Signal (AMS) / XADC | | | 0 | 0 | 1 | 1 | 1 | 1 |
| | Configuration AES / HMAC Blocks | | | 0 | 0 | 1 | 1 | 1 | 1 |
| Speed Grades | Commercial Temp (C) | | | -1,-2 | -1,-2 | -1,-2 | -1,-2 | -1,-2 | -1,-2 |
| | Industrial Temp (I) | | | -1,-2,-1L | -1,-2,-1L | -1,-2,-1L | -1,-2,-1L | -1,-2,-1L | -1,-2,-1L |
| | Expanded Temp (Q) | | | -1 | -1 | -1 | -1 | -1 | -1 |
| | Package ⁽¹⁾ | Body Area (mm) | Ball Pitch (mm) | Available User I/O: 3.3V SelectIO™ HR I/O | | | | | |
| | CPGA196 | 8x8 | 0.5 | 100 | 100 | | | | |
| | CSGA225 | 13x13 | 0.8 | 100 | 100 | 150 | | | |
| | CSGA324 | 15x15 | 0.8 | | | 150 | 210 | | |
| | FTGB196 | 15x15 | 1.0 | 100 | 100 | 100 | 100 | | |
| | FGGA484 | 23x23 | 1.0 | | | | 250 | 338 | 338 |
| | FGGA676 | 27x27 | 1.0 | | | | | 400 | 400 |

Notes:

1. Packages with the same last letter and number sequence, e.g., A484, are footprint compatible with all other Spartan 7 devices with the same sequence. The footprint compatible devices within this family are outlined.

Spartan™ 6 FPGAs

Spartan 6 LX FPGAs

I/O Optimization at the Lowest Cost
(1.2V, 1.0V)

Spartan 6 LXT FPGAs

I/O Optimization at the Lowest-Cost with Serial Connectivity (1.2V)

| Part Number | XC6SLX4 | XC6SLX9 | XC6SLX16 | XC6SLX25 | XC6SLX45 | XC6SLX75 | XC6SLX100 | XC6SLX150 | XC6SLX25T | XC6SLX45T | XC6SLX75T | XC6SLX100T | XC6SLX150T |
|--|-------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-------------|-------------|-------------|-------------|-------------|
| Slices ⁽¹⁾ | 600 | 1,430 | 2,278 | 3,758 | 6,822 | 11,662 | 15,822 | 23,038 | 3,758 | 6,822 | 11,662 | 15,822 | 23,038 |
| Logic Cells ⁽²⁾ | 3,840 | 9,152 | 14,579 | 24,051 | 43,661 | 74,637 | 101,261 | 147,443 | 24,051 | 43,661 | 74,637 | 101,261 | 147,443 |
| CLB Flip-Flops | 4,800 | 11,440 | 18,224 | 30,064 | 54,576 | 93,296 | 126,576 | 184,304 | 30,064 | 54,576 | 93,296 | 126,576 | 184,304 |
| Max. Distributed RAM (Kb) | 75 | 90 | 136 | 229 | 401 | 692 | 976 | 1,355 | 229 | 401 | 692 | 976 | 1,355 |
| Block RAM (18Kb each) | 12 | 32 | 32 | 52 | 116 | 172 | 268 | 268 | 52 | 116 | 172 | 268 | 268 |
| Total Block RAM (Kb) ⁽³⁾ | 216 | 576 | 576 | 936 | 2,088 | 3,096 | 4,824 | 4,824 | 936 | 2,088 | 3,096 | 4,824 | 4,824 |
| Clock Mgmt Tiles (CMT) ⁽⁴⁾ | 2 | 2 | 2 | 2 | 4 | 6 | 6 | 6 | 2 | 4 | 6 | 6 | 6 |
| Max. Single-Ended I/O Pins | 132 | 200 | 232 | 266 | 358 | 408 | 480 | 576 | 250 | 296 | 348 | 498 | 540 |
| Max. Differential I/O Pairs | 66 | 100 | 116 | 133 | 179 | 204 | 240 | 288 | 125 | 148 | 174 | 249 | 270 |
| DSP48A1 Slices ⁽⁵⁾ | 8 | 16 | 32 | 38 | 58 | 132 | 180 | 180 | 38 | 58 | 132 | 180 | 180 |
| Endpoint Block for PCIe® | — | — | — | — | — | — | — | — | 1 | 1 | 1 | 1 | 1 |
| Memory Controller Blocks | 0 | 2 | 2 | 2 | 2 | 4 | 4 | 4 | 2 | 2 | 4 | 4 | 4 |
| GTP Low-Power Transceivers | — | — | — | — | — | — | — | — | 2 | 4 | 8 | 8 | 8 |
| Commercial Speed Grade ⁽¹⁰⁾ | -1L, -2, -3 | -1L, -2, -3, -3N | -2, -3, -3N |
| Industrial Speed Grade ⁽¹⁰⁾ | -1L, -2, -3 | -1L, -2, -3, -3N | -2, -3, -3N |
| Configuration Memory (Mb) | 2.7 | 2.7 | 3.7 | 6.4 | 11.9 | 19.6 | 26.5 | 33.8 | 6.4 | 11.9 | 19.6 | 26.5 | 33.8 |

Maximum User I/O: SelectIO™ Interface Pins (GTP Transceivers)⁽⁶⁾

| Package | Body Area (mm) | Ball Pitch (mm) | XC6SLX4 | XC6SLX9 | XC6SLX16 | XC6SLX25 | XC6SLX45 | XC6SLX75 | XC6SLX100 | XC6SLX150 | XC6SLX25T | XC6SLX45T | XC6SLX75T | XC6SLX100T | XC6SLX150T |
|-------------------------|----------------|-----------------|---------|---------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|-----------|------------|------------|
| CPG196 ⁽⁷⁾ | 8 x 8 | 0.5 | 106 | 106 | 106 | | | | | | | | | | |
| TQG144 ⁽⁷⁾ | 20 x 20 | 0.5 | 102 | 102 | | | | | | | | | | | |
| CSG225 ⁽⁸⁾ | 13 x 13 | 0.8 | 132 | 160 | 160 | | | | | | | | | | |
| CSG324 | 15 x 15 | 0.8 | | 200 | 232 | 226 | 218 | | | | 190 (2) | 190 (4) | | | |
| CSG484 ⁽⁹⁾ | 19 x 19 | 0.8 | | | | | 320 | 328 | 338 | 338 | | 296 (4) | 292 (4) | 296 (4) | 296 (4) |
| FT(G)256 | 17 x 17 | 1.0 | | 186 | 186 | 186 | | | | | | | | | |
| FG(G)484 ⁽⁹⁾ | 23 x 23 | 1.0 | | | | 266 | 316 | 280 | 326 | 338 | 250 (2) | 296 (4) | 268 (4) | 296 (4) | 296 (4) |
| FG(G)676 | 27 x 27 | 1.0 | | | | | 358 | 408 | 480 | 498 | | | 348 (8) | 376 (8) | 396 (8) |
| FG(G)900 | 31 x 31 | 1.0 | | | | | | | | 576 | | | | 498 (8) | 540 (8) |

- Notes:
- Each slice contains four LUTs and eight flip-flops.
 - Spartan 6 FPGA logic cell ratings reflect the increased logic capacity offered by the 6-input LUT architecture.
 - Block RAM are fundamentally 18Kb in size. Each block can also be used as two independent 9 Kb blocks.
 - Each CMT contains two DCMs and one PLL.
 - Each DSP48A1 slice contains an 18x18 multiplier, an adder, and an accumulator.
 - The LX device pinouts are not compatible with the LXT device pinouts.
 - CPG196 and TQG144 do not have memory controller support. -3N is not available for these packages.
 - CSG225 has X8 memory controller support in the LX9 and LX16 devices. There is no memory controller in the LX4 devices.
 - Devices in the FG(G)484 and CSG484 packages have support for two memory controllers.
 - Devices with -3N speed grade do not support MCB functionality.

CoolRunner II CPLDs

High performance and ultra-low power consumption in a single-chip, instant-on programmable device (1.8V)

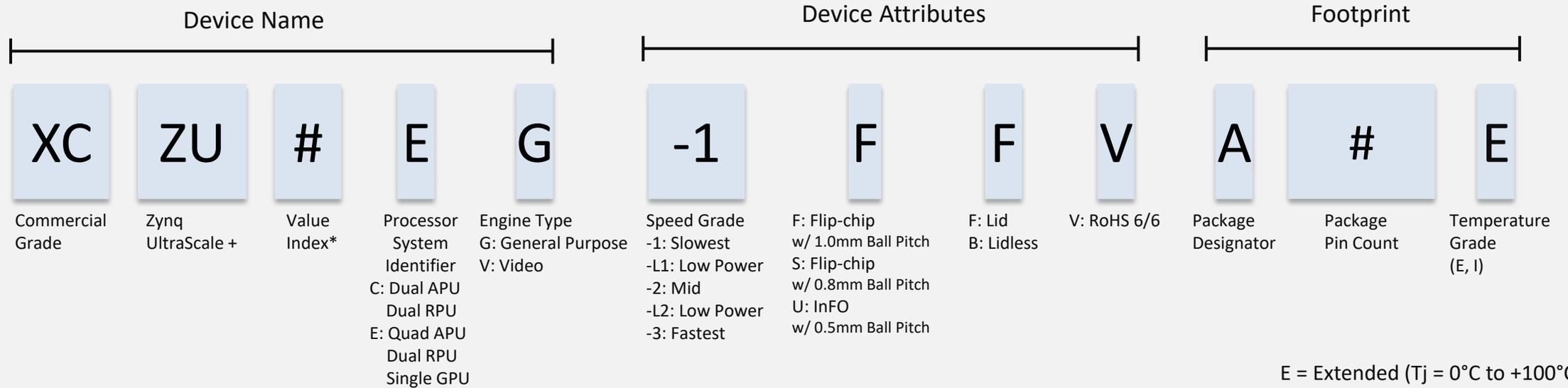
| | Part Number | XC2C32A | XC2C64A | XC2C128 | XC2C256 | XC2C384 | XC2C512 |
|-----------------|--|-----------------------|---------|---------|---------|---------|-------------------------|
| Logic Resources | System Gates | 750 | 1,500 | 3,000 | 6,000 | 9,000 | 12,000 |
| | Macrocells | 32 | 64 | 128 | 256 | 384 | 512 |
| | Product Terms Per Macrocell | 56 | 56 | 56 | 56 | 56 | 56 |
| Clock Resources | Global Clocks | 3 | 3 | 3 | 3 | 3 | 3 |
| | Product Term Clocks Per Function Block | 16 | 16 | 16 | 16 | 16 | 16 |
| I/O Resources | Maximum I/O | 33 | 64 | 100 | 184 | 240 | 270 |
| | Input Voltage Compatible | 1.5 / 1.8 / 2.5 / 3.3 | | | | | |
| | Output Voltage Compatible | 1.5 / 1.8 / 2.5 / 3.3 | | | | | |
| Speed Grades | Min. Pin-to-Pin Logic Delay (ns) | 3.8 | 4.6 | 5.7 | 5.7 | 7.1 | 7.1 |
| | Commercial Speed Grades (Fastest to Slowest) | -4, -6 | -5, -7 | -6, -7 | -6, -7 | -7, -10 | -7, -10 |
| | Industrial Speed Grades (Fastest to Slowest) | -6 | -7 | -7 | -7 | -10 | -7 ⁽¹⁾ , -10 |

| Package ^{(3), (4)} | Area (mm) | Maximum User I/Os | | | | | |
|---|----------------|-------------------|----|-----|-----|-----|-----|
| QFN Packages (QF): Quad, flat, no-lead (0.5mm lead spacing) | | | | | | | |
| QFG32 ⁽⁴⁾ | 5 x 5 | 21 | | | | | |
| QFG48 ⁽⁴⁾ | 7 x 7 | | 37 | | | | |
| VQFP Packages (VQ): Very thin QFP (VQ44: 0.8mm lead spacing, VQ100: 0.5mm lead spacing) | | | | | | | |
| VQG44 | 12 x 12 | 33 | 33 | | | | |
| VQG100 | 16 x 16 | | 64 | 80 | 80 | | |
| Chip Scale Packages (CP): Wire-bond, chip-scale, BGA (0.5mm ball spacing) | | | | | | | |
| CPG56 | 6 x 6 | 33 | 45 | | | | |
| CPG132 | 8 x 8 | | | 100 | 106 | | |
| TQFP Packages (TQ): Thin QFP (0.5mm lead spacing) | | | | | | | |
| TQG100 | 16 x 16 | | | | | | |
| TQG144 | 22 x 22 | | | 100 | 118 | 118 | |
| PQFP Packages (PQ): Wire-bond, plastic, QFP (0.5 mm lead spacing) | | | | | | | |
| PQG208 | 30.6 x 30.6 mm | | | | 173 | 173 | 173 |
| FBGA Packages (FT): Wire-bond, fine-pitch, thin BGA (1.0 mm ball spacing) | | | | | | | |
| FTG256 | 17 x 17 mm | | | | 184 | 212 | 212 |
| FBGA Packages (FG): Wire-bond, fine-pitch, BGA (1.0 mm ball spacing) | | | | | | | |
| FGG324 | 23 x 23 mm | | | | | 240 | 270 |

Notes:

- 7 speed grade is only available in FT(G)256 package.
- All packages are available in Pb-Free and RoHS6 compliant versions.
- Area dimensions for lead-frame product are inclusive of the leads.
- Only available in RoHS6 compliant and Halogen-free packages.

Zynq™ UltraScale+™ MPSoC Ordering Information

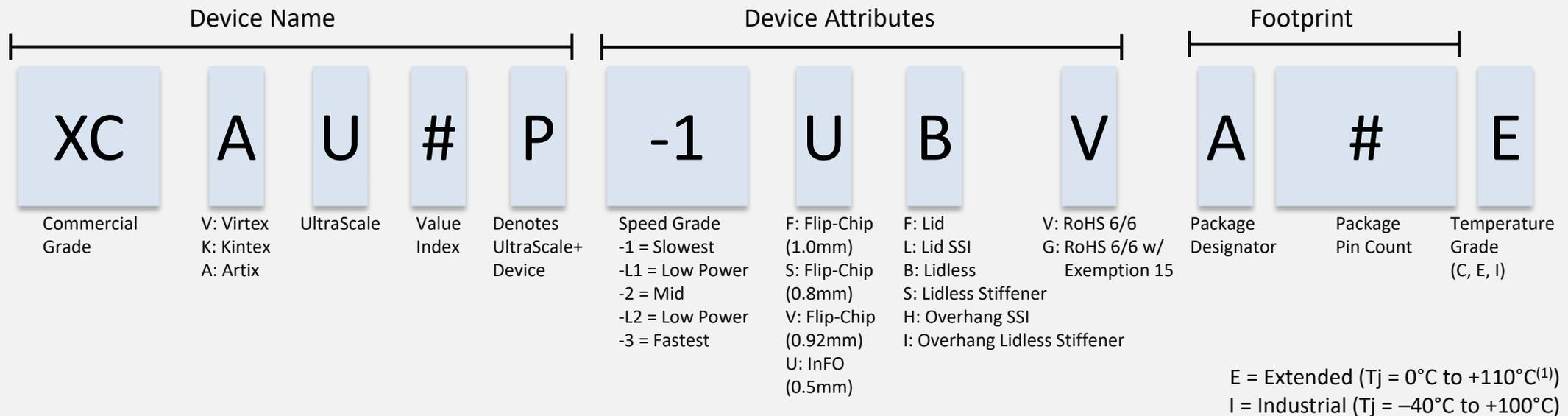


E = Extended (Tj = 0°C to +100°C)
I = Industrial (Tj = -40°C to +100°C)

*T in ZU3T value index denotes increase in resources and transceivers vs. ZU3.

Note: -L2E (Tj = 0°C to +110°C). Refer to DS891, Zynq UltraScale+ MPSoC Overview for additional information.

UltraScale+™ Device Ordering Information



Notes:

1. For more details on 110°C operation, see the Ordering Information section in DS890, *UltraScale Architecture and Product Overview*

Device Ordering Information



| | | | | | | | | | |
|-------------------|------------|----------|-------------|---|--|--|---|-------------------|-----------------------------|
| XC | 7 | Z | ### | S | -1 | FF | V | ### | C |
| Xilinx Commercial | Generation | Family | Value Index | Single Core Indicator (Z-7007S, Z-7012S, Z-7014S) | Speed Grade -1: Slowest -L1: Low Power -2: Mid -L2: Low Power -3: Fastest | Package Type CL: Wire-bond (.8mm) SB: Bare-die Flip-chip (.8mm) FB: Bare-die Flip-chip (1mm) FF: Flip-chip (1mm) | V: RoHS 6/6 G (CLG) = RoHS 6/6 G (SBG, FBG, FFG) = RoHS 6/6 with exemption 15 | Package Pin Count | Temperature Grade (C, E, I) |



| | | | | | | | | |
|-------------------|------------|----------|-------------------------|---|--|---|---------------------------|-----------------------------|
| XC | 7 | A | ### | -1 | FF | G | 900 | C |
| Xilinx Commercial | Generation | Family | Logic Cells In 1K units | Speed Grade -1 = Slowest -L1 = Low Power -L2 = Low Power -2 = Mid -3 = Highest | Package Type CP: Wire-bond (.5mm) CS: Wire-bond (.8mm) SB: Bare-die Flip-chip (.8mm) FT: Wire-bond (1mm) FG: Wire-bond (1mm) FB: Bare-die Flip-chip (1mm) FF: Flip-chip (1mm) | V: RoHS 6/6 G: RoHS 6/6 w/exemption 15 | Nominal Package Pin Count | Temperature Grade (C, E, I) |



| | | | | | | | | | |
|-------------------|------------|----------|-------------------------|--|--|-------------|--------------------|-------------------|-----------------------------|
| XC | 7 | S | ### | -1 | FG | G | A | 484 | C |
| Xilinx Commercial | Generation | Family | Logic Cells In 1K units | Speed Grade -1 = Slowest -L1 = Low Power -2 = Mid | Package Type CP: Wire-bond (.5mm) CS: Wire-bond (.8mm) FG: Wire-bond (1mm) FT: Wire-bond (1mm) | G: RoHS 6/6 | Package Designator | Package Pin Count | Temperature Grade (C, I, Q) |



| | | | | | | | | | |
|-------------------|------------|----------|---------------|-------------------------|--|---|-------------|-------------------|--------------------------|
| XC | 6 | S | LX LXT | ### | -1 | FB | G | 900 | C |
| Xilinx Commercial | Generation | Family | Sub-families | Logic Cells In 1K units | Speed Grade -L1 = Low Power -2 = Mid -3 = Highest -N3 = No MCB functionality | Package Type CP: Wire-bond (.5mm) TQ: Quad Flat Pack (.5mm) CS: Wire-bond (.8mm) FT: Wire-bond (1mm) FG: Wire-bond (1mm) | G: RoHS 6/6 | Package Pin Count | Temperature Grade (C, I) |

Notes:

-L1 is the ordering code for the lower power, -1L speed grade.

-L2 is the ordering code for the lower power, -2L speed grade.

C = Commercial (Tj = 0°C to +85°C) E = Extended (Tj = 0°C to +100°C) I = Industrial (Tj = -40°C to +100°C) Q = Expanded (Tj = -40°C to +125°C)

CPLD Device Ordering Information



XC2C128

Device

-4

Speed Grade
-4 thru -10
(Fastest to Slowest)

TQ

Package Type

QFN Packages (QF): Quad, flat, no-lead (0.5mm lead spacing)
VQFP Packages (VQ): Very thin QFP (VQ44: 0.8mm lead spacing, VQ100: 0.5mm lead spacing)
Chip Scale Packages (CP): Wire-bond, chip-scale, BGA (0.5mm ball spacing)
TQFP Packages (TQ): Thin QFP (0.5mm lead spacing)
FBGA Packages (FG): Wire-bond, fine-pitch, BGA (1.0mm ball spacing)
FBGA Packages (FT): Wire-bond, fine-pitch, thin BGA (1.0mm ball spacing)

G

Pb-Free

144

Pin
Count

C

Temperature
Grade
(C, I)

Notes:

C = Commercial ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$) I = Industrial ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Important: Verify all data in this document with the device data sheets.

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