UltraScale+ FPGAs
Product Tables and Product Selection Guide

ARTIX UltraSCALE+ KINTEX UltraSCALE+ VIRTEX UltraSCALE+

AMD XILINX

Artix® UltraScale+™ FPGAs

Device Name	AU7P	AU10P	AU15P	AU20P	AU25P
System Logic Cells (K)	82	96	170	238	308
CLB Flip-Flops (K)	75	88	156	218	282
CLB LUTs (K)	37	44	78	109	141
Dist. RAM (Mb)	1.1	1.0	2.5	3.2	4.7
Total Block RAM (Mb)	3.8	3.5	5.1	7.0	10.5
36K Block RAM Blocks	108	100	144	200	300
UltraRAM (Mb)	–	–	–	–	–
Clock Management Tiles (CMTs)	2	3	3	3	4
DSP Slices	216	400	576	900	1,200
PCI Express®	1x Gen3x4	1x Gen4x8(1)	1x Gen4x8(1)	1x Gen3x8	1x Gen3x8
AMS - System Monitor	1	1	1	1	1
Max. Single-Ended HD I/Os	144	72	72	72	96
Max. Single-Ended HP I/Os	104	156	156	156	208
GTH Transceivers(2)	4	12	12	–	–
GTY Transceivers(2)	–	–	–	12	12
Extended			-1 -2		
Industrial			-1 -2 -1L		

Package	Dim. (mm)	Ball Pitch (mm)	HD I/O, HP I/O, GTH, GTY				
UBVA368	11.5x9.5	0.5		24, 104, 8, 0	24, 104, 8, 0		
SBVB484	19x19	0.8		48, 156, 12, 0	48, 156, 12, 0		
SBVC484	19x19	0.8	144, 104, 4, 0				
SFVB784	23x23	0.8				72, 156, 0, 12	96, 208, 0, 12
FFVB676	27x27	1.0		72, 156, 12, 0	72, 156, 12, 0	72, 156, 0, 12	72, 208, 0, 12

Notes:
1. PCIe Gen4 is available in AU10P and AU15P in the FFVB676 package. AU10P and AU15P in other packages support Gen3x8.
2. GTH and GTY data rates are package dependent:
- Maximum 12.5Gb/s in UBVA292, UBVA368, SBVB484, SBVC484, SFVB784
- Maximum 16.3Gb/s in FFVB676.

Kintex® UltraScale+™ FPGAs

	Device Name	KU3P	KU5P	KU9P	KU11P	KU13P	KU15P	KU19P
Logic	System Logic Cells (K)	356	475	600	653	747	1,143	1,843
	CLB Flip-Flops (K)	325	434	548	597	683	1,045	1,685
	CLB LUTs (K)	163	217	274	299	341	523	842
Memory	Max. Distributed RAM (Mb)	4.7	6.1	8.8	9.1	11.3	9.8	11.6
	Total Block RAM (Mb)	12.7	16.9	32.1	21.1	26.2	34.6	60.8
	UltraRAM (Mb)	13.5	18.0	0	22.5	31.5	36.0	81.0
Clocking	Clock Mgmt Tiles (CMTs)	4	4	4	8	4	11	9
Integrated IP	DSP Slices	1,368	1,824	2,520	2,928	3,528	1,968	1,080
	PCIE4 (PCIe® Gen3 x16)	1	1	0	4	0	5	0
	PCIE4C (PCIe® Gen3 x16 / Gen4 x8 /CCIX)	0	0	0	0	0	0	3
	150G Interlaken	0	0	0	1	0	4	0
	100G Ethernet w/ KR4 RS-FEC	0	1	0	2	0	4	1
I/O	Max. Single-Ended HD I/Os	96	96	96	96	96	96	72
	Max. Single-Ended HP I/Os	208	208	208	416	208	572	468
	GTH 16.3Gb/s Transceivers	0	0	28	32	28	44	0
	GTY 32.75Gb/s Transceivers	16	16	0	20	0	32	32
Speed Grades	Extended[1]	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3
	Industrial	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2

Footprint compatible with 20nm UltraScale Devices with same footprint identifier								
Footprint[2, 3]	Dimensions (mm)	HD I/O, HP I/O, GTH 16.3Gb/s, GTY 32.75Gb/s						
B784[4]	23x23[5]	96, 208, 0, 16	96, 208, 0, 16					
A676[4]	27x27	48, 208, 0, 16	48, 208, 0, 16					
B676	27x27	72, 208, 0, 16	72, 208, 0, 16					
D900[4]	31x31	96, 208, 0, 16	96, 208, 0, 16		96, 312, 16, 0			
E900	31x31			96, 208, 28, 0		96, 208, 28, 0		
A1156[4]	35x35				48, 416, 20, 8		48, 468, 20, 8	
E1517	40x40				96, 416, 32, 20		96, 416, 32, 24	
A1760	42.5x42.5						96, 416, 44, 32	
E1760	42.5x42.5						96, 572, 32, 24	
J1760	42.5x42.5							72, 468, 0, 32
B2104	47.5x47.5							72, 468, 0, 32

1. -2LE (Tj = 0°C to 110°C). For more details, see the Ordering Information section in DS890, UltraScale Architecture and Product Overview.
2. Maximum achievable performance is device and package dependent; consult the associated data sheet for details.
3. For full part number details, see the Ordering Information section in DS890, *UltraScale Architecture and Product* Overview.
4. GTY transceiver line rates are package limited: B784 to 12.5Gb/s; A676, D900, and A1156 to 16.3Gb/s. Refer to data sheet for details.
5. The B784 package is only offered in 0.8mm ball pitch. All other packages are 1.0mm ball pitch.

Virtex® UltraScale+™ FPGAs

			Foundation						58G PAM4		
	Device Name		VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU19P	VU23P	VU27P	VU29P
	System Logic Cells (K)		862	1,314	1,724	2,586	2,835	3,780	8,938	2,252	2,835	3,780
	CLB Flip-Flops (K)		788	1,201	1,576	2,364	2,592	3,456	8,172	2,059	2,592	3,456
	CLB LUTs (K)		394	601	788	1,182	1,296	1,728	4,086	1,030	1,296	1,728
	Max. Dist. RAM (Mb)		12.0	18.3	24.1	36.1	36.2	48.3	58.4	14.2	36.2	48.3
	Total Block RAM (Mb)		25.3	36.0	50.6	75.9	70.9	94.5	75.9	74.3	70.9	94.5
	UltraRAM (Mb)		90.0	132.2	180.0	270.0	270.0	360.0	90.0	99.0	270.0	360.0
	DSP Slices		2,280	3,474	4,560	6,840	9,216	12,288	3,840	1,320	9,216	12,288
	Peak INT8 DSP (TOP/s)		7.1	10.8	14.2	21.3	28.7	38.3	10.4	4.1	28.7	38.3
	PCIe® Gen3 x16		2	4	4	6	3	4	0	0	1	1
	PCIe Gen3 x16/Gen4 x8 / CCIX[1]		–	–	–	–	–	–	8	4	–	–
	150G Interlaken		3	4	6	9	6	8	0	0	8	8
	100G Ethernet w/ KR4 RS-FEC		3	4	6	9	9	12	0	2	15	15
	Max. Single-Ended HP I/Os		520	832	832	832	624	832	1,976	572	676	676
	Max. Single-Ended HD I/Os		0	0	0	0	0	0	96	72	0	0
	GTY 32.75Gb/s Transceivers		40	80	80	120	96	128	80	34	32	32
	GTM 58Gb/s PAM4 Transceivers		–	–	–	–	–	–	–	4	48	48
	100G / 50G KP4 FEC		–	–	–	–	–	–	–	2 / 4	24 / 48	24 / 48
	Extended[2]		-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3
	Industrial		-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	–	-1, -2	-1 -2	-1 -2
	Footprint[3,4,5]	Dim. (mm)	HP I/O, GTY						HP I/O, HD I/O, GTY	HP I/O, HD I/O, GTY, GTM		
Footprint compatible with 20nm UltraScale Devices with same footprint identifier	A1365[4]	35x35								364, 0, 34[8], 4		
	C1517	40x40	520, 40									
	J1760	42.5x42.5								572, 72, 34, 4		
	F1924[6]	45x45					624, 64					
	A2104	47.5x47.5		832, 52	832, 52	832, 52						
		52.5x52.5[7]						832, 52				
	B2104	47.5x47.5		702, 76	702, 76	702, 76	572, 76					
		52.5x52.5[7]						702, 76				
	C2104	47.5x47.5		416, 80	416, 80	416, 104	416, 96					
		52.5x52.5[7]						416, 104				
	D2104	47.5x47.5				676, 76	572, 76					
		52.5x52.5[7]						676, 76			676, 16, 30	676, 16, 30
	H2104	47.5x47.5										
	A2577	52.5x52.5				448, 120	448, 96	448, 128			448, 32, 48	448, 32, 48
	A3824	65x65							1976, 96,48			
	B3824	65x65							1664, 96, 80			

1. This block operates in compatibility mode for 16.0GT/s (Gen4) operation. See PG213.
2. -2LE (Tj = 0°C to 110°C). See Ordering Information in DS890.
3. For full part number details, see DS890, *UltraScale Architecture and Product Overview*.
4. All packages are 1.0mm ball pitch, with the exception of A1365, which is 0.92mm.
5. Consult UG583, *UltraScale Architecture PCB Design User Guide* for specific migration details.
6. The GTY transceiver line rate in the F1924 footprint is package limited to 16.3Gb/s. Refer to data sheet for details.
7. These 52.5x52.5mm packages have the same PCB ball footprint as the 47.5x47.5mm packages and are footprint compatible.
8. GTYs in quads 224-230 and 232 are limited to 16Gb/s.

XMP103 (v2.2)

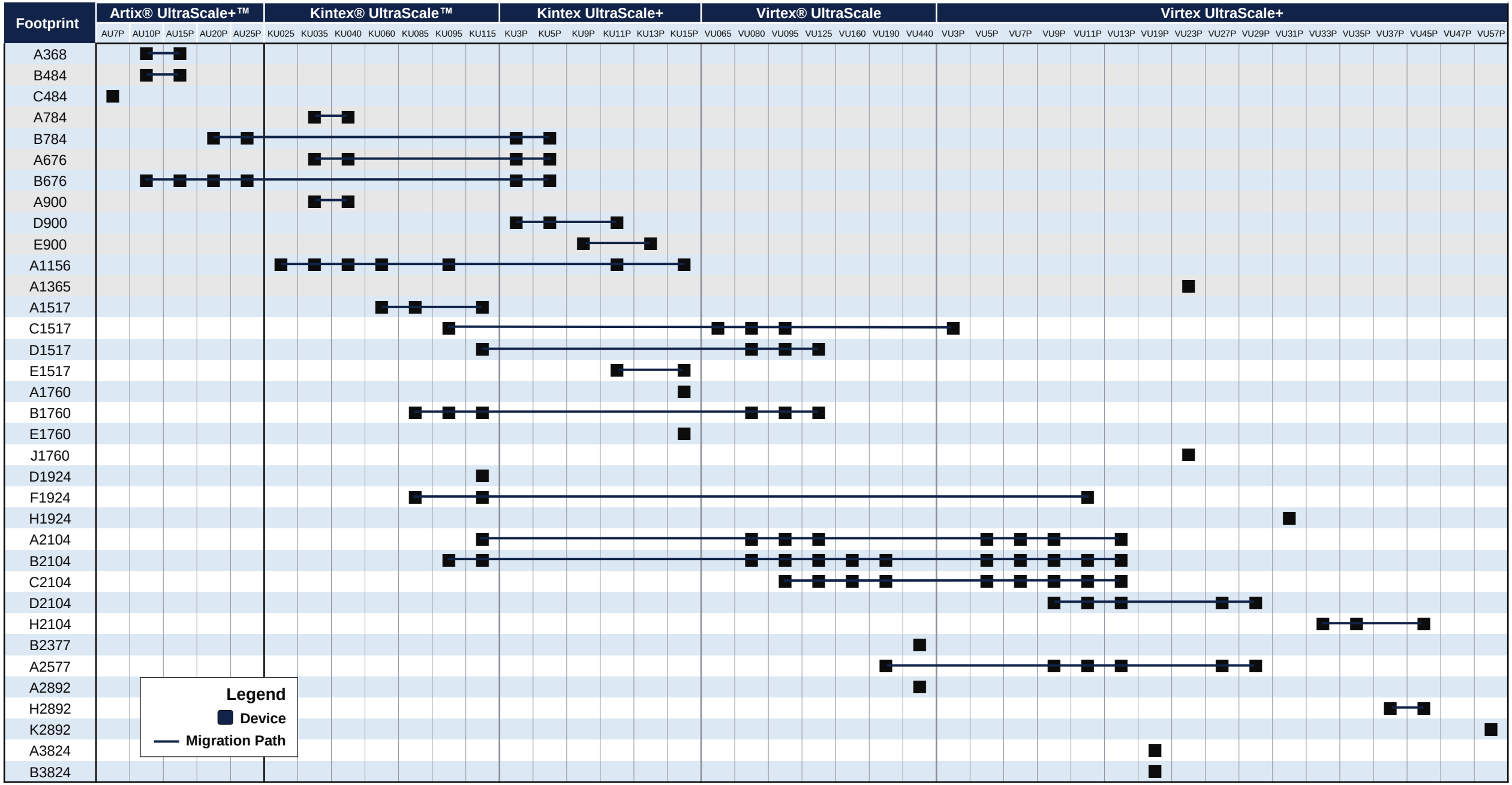
AMD XILINX

	HBM (4GB)	HBM (8GB)			HBM (16GB)		
Device Name	VU31P	VU33P	VU35P	VU37P	VU45P	VU47P	VU57P
System Logic Cells (K)	962	962	1,907	2,852	1,907	2,852	2,852
CLB Flip-Flops (K)	879	879	1,743	2,607	1,743	2,607	2,607
CLB LUTs (K)	440	440	872	1,304	872	1,304	1,304
Max. Dist. RAM (Mb)	12.5	12.5	24.6	36.7	24.6	36.7	36.7
Total Block RAM (Mb)	23.6	23.6	47.3	70.9	47.3	70.9	70.9
UltraRAM (Mb)	90.0	90.0	180.0	270.0	180.0	270.0	270.0
HBM DRAM (GB)	4	8	8	8	16	16	16
HBM AXI Interfaces	16	32	32	32	32	32	32
Clock Mgmt Tiles (CMTs)	4	4	8	12	8	12	12
DSP Slices	2,880	2,880	5,952	9,024	5,952	9,024	9,024
Peak INT8 DSP (TOP/s)	8.9	8.9	18.6	28.1	18.6	28.1	28.1
PCIe® Gen3 x16	0	0	1	2	1	2	0
PCIe Gen3 x16/Gen4 x8 / CCIX[1]	4	4	4	4	4	4	4
150G Interlaken	0	0	2	4	2	4	4
100G Ethernet w/ KR4 RS-FEC	2	2	5	8	5	8	10
Max. Single-Ended HP I/Os	208	208	416	624	416	624	624
GTY 32.75Gb/s Transceivers	32	32	64	96	64	96	32
GTM 58Gb/s PAM4 Transceivers	–	–	–	–	–	–	32
100G / 50G KP4 FEC	–	–	–	–	–	–	16/32
Extended[2]	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3
Industrial	–	–	–	–	–	–	–

Footprint[3, 4, 5, 6]	Dim. (mm)	HP I/O, GTY					HP I/O, GTY, GTM
H1924	45x45	208, 32					
H2104	47.5x47.5		208, 32	416, 64		416, 64	
H2892	55x55			416, 64	624, 96	416, 64	624, 96
K2892	55x55						624, 32, 32

1. This block operates in compatibility mode for 16.0GT/s (Gen4) operation. See PG213.
2. -2LE (Tj = 0°C to 110°C). See Ordering Information in DS890.
3. For full part number details, see DS890, *UltraScale Architecture and Product Overview*.
4. All packages are 1.0mm ball pitch.
5. Consult UG583, *UltraScale Architecture PCB Design User Guide* for specific migration details.
6. Footprint compatible with 20nm UltraScale Devices with same footprint identifier.

UltraScale Architecture Migration Table



UltraScale+ Device Ordering Information

Device Name					Device Attributes				Footprint		
XC	V	U	#	P	-1	F	L	V	A	#	E
Commercial Grade	V: Virtex K: Kintex A: Artix	UltraScale	Value Index	Denotes UltraScale+ Device	Speed Grade -1 = Slowest -L1 = Low Power -2 = Mid -L2 = Low Power -3 = Fastest	F: Flip-Chip (1.0mm) S: Flip-Chip (0.8mm) V: Flip-Chip (0.92mm) U: InFO (0.5mm)	F: Lid L: Lid SSI B: Lidless S: Lidless Stiffener H: Overhang SSI I: Overhang Lidless Stiffener	V: RoHS 6/6 G: RoHS 6/6 w/ Exemption 15	Package Designator	Package Pin Count	Temperature Grade (E, I)

E = Extended (Tj = 0°C to +110°C(1))
I = Industrial (Tj = –40°C to +100°C)

Notes:
1. For more details on 110°C operation, see the Ordering Information section in DS890, *UltraScale Architecture and Product Overview*

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