Product roadmap

RAM solutions

Q1 2023

Cypress Semiconductor Corp.
An Infineon Technologies Company

Table of Contents

Nonvolatile RAM

F-RAM, nvSRAM

F-RAM portfolio

Low power | High endurance

	LPC[1] F-RAM				Processor Companion	Parallel F-RAM	
512Kb–16Mb	**FM25V20A** **2Mb**; 2.0–3.6 V 40-MHz SPI; Ind[2]	**CY15B104Q** **4Mb;** 2.0–3.6 V 40-MHz SPI; Ind	**EXCELON™ [3] F-RAM** **Up to 16Mb** **1.8 V, 108-MHz QSPI[4]**			**FM22L16/LD16** **4Mb**; 2.7–3.6 V 55 ns; x8; Ind	
	FM25V10/VN10 **1Mb**; 2.0–3.6 V 40-MHz SPI; Ind	**CY15B102Q** **2Mb;** 2.0–3.6 V 25-MHz SPI; Auto E[6]	**FM24V10/VN10** **1Mb**; 2.0–3.6 V 3.4-MHz I²C; Ind			**FM28V102A** **1Mb;** 2.0–3.6 V 60 ns; x16; Ind	**FM28V202A** **2Mb;** 2.0–3.6 V 60 ns; x16; Ind
	FM25V05 **512Kb**; 2.0–3.6 V 40-MHz SPI; Ind		**FM24V05** **512Kb**; 2.0–3.6 V 3.4-MHz I²C; Ind			**CY15B101N** **1Mb;** 2.0–3.6 V 60 ns; x16; Auto A, E	**CY15B102N** **2Mb;** 2.0–3.6 V 60 ns; x16; Auto A, E
4–256Kb	**FM25V02A/W256** **256Kb**; V02A: 2.0–3.6 V W256: 2.7–5.5 V 40-MHz SPI; Ind	**CY15B256Q** **256Kb**; 3.3V 33/40-MHz SPI; Auto A[5], E	**FM24V02A/W256** **256Kb**; V02A: 2.0–3.6 V W256: 2.7–5.5 V 3.4-MHz I²C; Ind	**CY15B256J** **256Kb**; 2.0–3.6 V 3.4-MHz I²C; Auto A, E	**FM33256** Q323 **256Kb**; 3.3 V; 16-MHz SPI Ind; RTC[7]; Power Fail Watchdog; Counter	**FM28V020** **256Kb**; 2.0–3.6 V 70 ns; x8; Ind	**FM18W08** **256Kb**; 2.7–5.5 V 70 ns; x8; Ind
	FM25V01A **128Kb**; 2.0–3.6 V 40-MHz SPI; Ind	**CY15B128Q** **128Kb**; 3.3V 33/40-MHz SPI; Auto A, E	**FM24V01A** **128Kb**; 2.0–3.6 V 3.4-MHz I²C; Ind	**CY15B128J** **128Kb**; 2.0–3.6 V 3.4-MHz I²C; Auto A, E	**FM31256/31(L)278** **256Kb**; 3.3, 5.0 V; 1-MHz I²C; Ind; RTC; Power Fail; Watchdog; Counter	**FM1808B** **256Kb**; 5.0 V 70 ns; x8; Ind	**FM16W08** **64Kb**; 2.7–5.5 V 70 ns; x8; Ind
	FM25640B/CL64B **64Kb**; 3.3, 5.0 V 20-MHz SPI; Ind	**CY15B064Q/E064Q** **64Kb**; 3.3, 5.0 V 16/20-MHz SPI; Auto A, E	**FM24C64/CL64** **64Kb**; 3.3, 5.0 V 1-MHz I²C; Ind	**CY15B064J/E064J** **64Kb**; 3.3, 5.0 V 1-MHz I²C; Auto A, E	**FM3164/31(L)276** **64Kb**; 3.3, 5.0 V; 1-MHz I²C; Ind; RTC; Power Fail; Watchdog; Counter		
	FM25C160/L16 **16Kb**; 3.3, 5.0 V 20-MHz SPI; Ind	**CY15B016Q/E016Q** **16Kb**; 3.3, 5.0 V 16/20-MHz SPI; Auto A, E	**FM24C16/CL16** **16Kb**; 3.3, 5.0 V 1-MHz I²C; Ind	**CY15B016J/E016J** **16Kb**; 3.3, 5.0 V 1-MHz I²C; Auto A, E			
	FM25040/L04 **4Kb**; 3.3, 5.0 V 20-MHz SPI; Ind	**CY15B004Q/E004Q** **4Kb**; 3.3, 5.0 V 16/20-MHz SPI; Auto A, E	**FM24C04/CL04** **4Kb**; 3.3, 5.0 V 1-MHz I²C; Ind	**CY15B004J/E004J** **4Kb**; 3.3, 5.0 V 1-MHz I²C; Auto A, E			

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY
EOL (Last-Time-Ship)				QQYY
Automotive				

[1] Low-pin-count
[2] Industrial grade -40 °C to +85 °C
[3] Ultra-low-energy
[4] Quad serial peripheral interface
[5] AEC-Q100 -40 °C to +85 °C
[6] AEC-Q100 -40 °C to +125 °C

EXCELON™ F-RAM portfolio

Ultra low power | High speed | High endurance

	EXCELON™ Auto		EXCELON™ Ultra		EXCELON™ LP	
1Mb – 16Mb	**CY15B116QSN** Q223 **16Mb;** 1.8–3.6 V 24-ball FBGA 108-MHz QSPI[1] Auto S[2]	**CY15V116QSN** Q223 **16Mb;** 1.71–1.89 V 24-ball FBGA 108-MHz QSPI Auto S	**CY15B116QSN** **16Mb**; 1.8–3.6 V 24-ball FBGA 108-MHz QSPI, Ind[3], Ind Q	**CY15V116QSN** **16Mb**; 1.71–1.89 V 24-ball FBGA 108-MHz QSPI, Ind, Ind Q	**CY15B116QI/N** **16Mb**; 1.8–3.6 V 24-ball FBGA 20/40-MHz SPI, Comm[4], Ind	**CY15V116QI/N** **16Mb**; 1.71–1.89 V 24-ball FBGA 20/40-MHz SPI, Comm, Ind
	CY15B116QN **16Mb;** 1.8–3.6 V 24-ball FBGA 40-MHz SPI; Auto A[5]	**CY15V116QN** **16Mb;** 1.71–1.89 V 24-ball FBGA 40-MHz SPI; Auto A				
	CY15B108QSN Q223 **8Mb;** 1.8–3.6 V 24-ball FBGA 108-MHz QSPI; Auto S	**CY15V108QSN** Q223 **8Mb;** 1.71–1.89 V 24-ball FBGA 108-MHz QSPI; Auto S	**CY15B108QSN** **8Mb**; 1.8–3.6 V 24-ball FBGA 108-MHz QSPI, Ind, Ind Q	**CY15V108QSN** **8Mb**; 1.71–1.89 V 24-ball FBGA 108-MHz QSPI, Ind, Ind Q	**CY15B108QN** **8Mb**; 1.8–3.6 V 24-ball FBGA 50-MHz SPI, Ind, Ind Q[7]	**CY15V108QN** **8Mb**; 1.71–1.89 V 24-ball FBGA 50-MHz SPI, Ind, Ind Q
	CY15B208QN **8Mb;** 1.8–3.6 V 24-ball FBGA 40-MHz SPI; Auto E[6]	**CY15V208QN** **8Mb;** 1.71–1.89 V 24-ball FBGA 40-MHz SPI; Auto E	**CY15B108QSN** **8Mb**; 1.8–3.6 V 8-pin GQFN, SOIC 108-MHz QSPI, Ind	**CY15V108QSN** **8Mb**; 1.71–1.89 V 8-pin GQFN, SOIC 108-MHz QSPI, Ind	**CY15B108QI/N** **8Mb**; 1.8–3.6 V 8-pin GQFN 20/40-MHz SPI, Comm, Ind	**CY15V108QI/N** **8Mb**; 1.71–1.89 V 8-pin GQFN 20/40-MHz SPI, Comm, Ind
	CY15B204QN **4Mb;** 1.8–3.6 V 8-pin SOIC 40-MHz SPI; Auto E	**CY15V204QN** **4Mb;** 1.71–1.89 V 8-pin SOIC 40-MHz SPI; Auto E				
	CY15B104QN **4Mb;** 1.8–3.6 V 8-pin SOIC 50-MHz SPI; Auto A	**CY15V104QN** **4Mb;** 1.71–1.89 V 8-pin SOIC 50-MHz SPI; Auto A	**CY15B104QSN** **4Mb**; 1.8–3.6 V 8-pin GQFN, SOIC 108-MHz QSPI, Ind	**CY15V104QSN** **4Mb**; 1.71–1.89 V 8-pin GQFN, SOIC 108-MHz QSPI, Ind	**CY15B104QI/N** **4Mb**; 1.8–3.6 V 8-pin GQFN, SOIC 20/50-MHz SPI, Comm, Ind	**CY15V104QI/N** **4Mb**; 1.71–1.89 V 8-pin GQFN, SOIC 20/50-MHz SPI, Comm, Ind
	CY15B102QN **2Mb;** 1.8–3.6 V 8-pin SOIC 50-MHz SPI; Auto E	**CY15V102QN** **2Mb;** 1.71–1.89 V 8-pin SOIC 50-MHz SPI; Auto E	**CY15B102QSN** **2Mb**; 1.8–3.6 V 8-pin SOIC 108-MHz QSPI, Ind	**CY15V102QSN** **2Mb**; 1.71–1.89 V 8-pin SOIC 108-MHz QSPI, Ind	**CY15B102QN/QM** **2Mb**; 1.8–3.6 V 8-pin DFN, SOIC 50-MHz SPI, Ind	**CY15V102QN** **2Mb**; 1.71–1.89 V 8-pin DFN, SOIC 50-MHz SPI, Ind
	CY15B201QN **1Mb;** 1.8–3.6 V 8-pin SOIC 50-MHz SPI; Auto E	**CY15V201QN** **1Mb;** 1.71–1.89 V 8-pin SOIC 50-MHz SPI; Auto E				

[1] Quad serial peripheral interface
[2] AEC-Q100 -40 °C to +105 °C
[3] Industrial grade -40 °C to +85 °C [4] Commercial grade 0 °C to +70 °C
[5] AEC-Q100 -40 °C to +85 °C
[6] AEC-Q100 -40 °C to +125 °C
[7] Industrial Q grade -40 °C to +105 °C

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY
EOL (Last-Time-Ship)				QQYY
Automotive				

EXCELON™ F-RAM roadmap

Product Family	Density (Prod) [EOL]	2020				2021				2022				2023				2024				2025				2026			
		Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
EXCELON™ Ultra F-RAM with serial Quad SPI interface	2Mb																												
	4Mb																												
	8Mb																												
	16Mb																												
EXCELON™ Auto F-RAM with serial SPI and Quad SPI interface AEC-Q100 qualified	1Mb																												
	2Mb																												
	4Mb																												
	8Mb (Q223)																												
	16Mb																												
EXCELON™ LP F-RAM with serial SPI interface Inrush[1] control	2Mb																												
	4Mb																												
	8Mb																												
	16Mb																												

[1] Switch-on surge current

Concept Samples Production EOL

F-RAM packages

Family	Density	8-pin SOIC	8-pin DFN	8-pin GQFN	8-pin EIAJ	14-pin SOIC	28-pin SOIC	28-pin TSOP I	32-pin TSOP I	44-pin TSOP II	24-ball FBGA	48-ball FBGA	Wafer
SPI	4Kb	✓	✓										
	16Kb	✓	✓										
	64Kb	✓	✓										
	128Kb	✓											
	256Kb	✓	✓										
	512Kb	✓											
	1Mb	✓			✓								
	2Mb	✓	✓		✓								
	4Mb		✓	✓	✓								
	8Mb			✓	✓						✓		
	16Mb										✓		
I^2C	4Kb	✓											
	16Kb	✓	✓										
	64Kb	✓	✓										
	128Kb	✓											
	256Kb	✓											
	512Kb	✓											
	1Mb	✓											
Processor Companion	64Kb					✓							
	256Kb					✓							
Parallel	64Kb						✓						
	256Kb						✓	✓	✓				✓
	1Mb								✓	✓			✓
	2Mb									✓			✓
	4Mb									✓		✓	

EXCELON™ F-RAM family overview

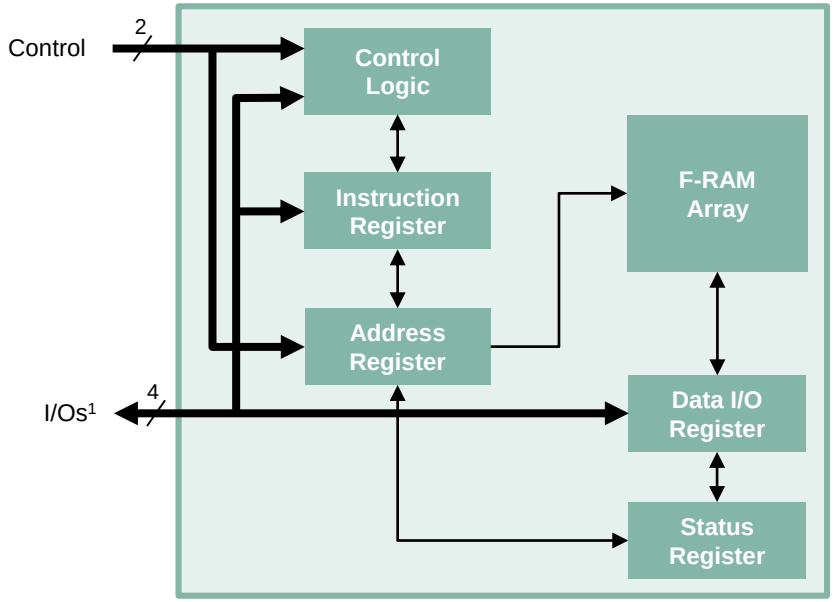
Applications

Medical devices, wearables, industrial control and automation, and automotive

Features

- **EXCELON™ Ultra**
  - 2Mb to 16Mb
  - 54-MHz Double Data Rate (DDR)/108-MHz Single Data Rate (SDR) Quad SPI
  - Industrial temperature range grade “I”: -40 ºC to +85 ºC
  - Industrial temperature range grade “Q”: -40 ºC to +105 ºC
- **EXCELON™ Auto**
  - 4Mb to 16Mb Auto “A”, 8Mb to 16Mb Auto “S”, 1Mb to 8Mb Auto “E”
  - 54-MHz Double Data Rate (DDR)/108-MHz Single Data Rate (SDR) Quad SPI
  - 40/50-MHz Serial Peripheral Interface (SPI)
  - Automotive temperature range grade “A”: -40 ºC to +85 ºC
  - Automotive temperature range grade “S”: -40 ºC to +105 ºC
  - Automotive temperature range grade “E”: -40 ºC to +125 ºC
- **EXCELON™ LP**
  - 2Mb to 16Mb
  - 20-MHz SPI (Commercial/Industrial), 40/50-MHz SPI (Industrial)
  - Ultra low (0.75 µA) deep power down current
  - Ultra low (0.1 µA) hibernate current
  - Commercial temperature range grade “C”: 0 °C to +70 °C
  - Industrial temperature range grade “I”: -40 °C to +85 °C
  - Industrial temperature range grade “Q”: -40 ºC to +105 ºC
- **Common features for EXCELON™ Ultra/Auto/LP**
  - Operating voltage ranges: 1.71 V to 1.89 V, 1.80 V to 3.60 V
  - 100-trillion read/write cycle endurance & 100-year data retention

EXCELON™ F-RAM



Family Table

Density	Standby Current (Typ.)	Active Current (Typ.)	Packages
1Mb[2]	3.2 µA	6.0 mA	SOIC (8)
2Mb	2.3 µA	2.4 mA	SOIC (8), TDFN (8)
4Mb	2.3 µA	2.4 mA	SOIC (8), GQFN (8)
8Mb	3.5 µA	2.6 mA	SOIC (8), GQFN (8), FBGA (24)
16Mb	8.0 µA	2.7 mA	FBGA (24)

[1] Quad SPI has 4 I/Os

[2] 1Mb density will be available in Automotive grade-E

F-RAM packages

Family	Density	8-pin SOIC	8-pin DFN	8-pin GQFN	8-pin EIAJ	14-pin SOIC	28-pin SOIC	28-pin TSOP I	32-pin TSOP I	44-pin TSOP II	24-ball FBGA	48-ball FBGA	Wafer
SPI	4Kb	✓	✓										
	16Kb	✓	✓										
	64Kb	✓	✓										
	128Kb	✓											
	256Kb	✓	✓										
	512Kb	✓											
	1Mb	✓											
	2Mb	✓	✓		✓								
	4Mb		✓	✓	✓								
	8Mb			✓	✓						✓		
	16Mb										✓		
I^2C	4Kb	✓											
	16Kb	✓	✓										
	64Kb	✓	✓										
	128Kb	✓											
	256Kb	✓											
	512Kb	✓											
	1Mb	✓											
Processor Companion	64Kb					✓							
	256Kb					✓							
Parallel	64Kb						✓						
	256Kb						✓	✓	✓				✓
	1Mb								✓	✓			✓
	2Mb									✓			✓
	4Mb									✓		✓	

nvSRAM portfolio
High density | High speed

	Parallel nvSRAM				LPC[1] nvSRAM			
512Kb–16Mb	**CY14B116R/S** **16Mb**; 3.0 V 25, 45 ns; x32; Ind[2] RTC[3]	**CY14B116K/L** **16Mb**; 3.0 V 25, 45 ns; x8; Ind RTC	**CY14V116F/G** **16Mb**; 3.0, 1.8 V I/O 30 ns; ONFI[4] 1.0 x8, x16; Ind					
	CY14B104NA **4Mb**; 3.0 V 25, 45 ns; x16 Auto E[6]; RTC	**CY14B108K/L** **8Mb**; 3.0 V 25, 45 ns; x8; Ind RTC	**CY14B108M/N** **8Mb**; 3.0 V 25, 45 ns; x16; Ind RTC	**CY14B116M/N** **16Mb**; 3.0 V 25, 45 ns; x16; Ind RTC				
	CY14B104K/LA **4Mb**; 3.0 V 25, 45 ns; x8; Ind RTC	**CY14V104LA** **4Mb**; 3.0, 1.8 V I/O 25, 45 ns; x8; Ind	**CY14B104M/NA** **4Mb**; 3.0 V 25, 45 ns; x16; Ind RTC	**CY14V104NA** **4Mb**; 3.0, 1.8 V I/O 25, 45 ns; x16; Ind	**CY14V101PS** **1Mb;** 3.0, 1.8 V I/O 108-MHz QSPI; Ind Ext. Ind[8]; RTC	**CY14V101QS** **1Mb;** 3.0, 1.8 V I/O 108-MHz QSPI; Ind Ext. Ind	**CY14B101I** **1Mb**; 3.0 V 3.4-MHz I²C; Ind RTC	
	CY14B101KA/LA **1Mb**; 3.0 V 25, 45 ns; x8; Ind RTC	**CY14V101LA** **1Mb**; 3.0, 1.8 V I/O 25, 45 ns; x8; Ind	**CY14B101MA/NA** **1Mb**; 3.0 V 25, 45 ns; x16; Ind RTC	**CY14V101NA** **1Mb**; 3.0, 1.8 V I/O 25, 45 ns; x16; Ind	**CY14B101PA** **1Mb**; 3.0 V 40-MHz SPI; Ind RTC	**CY14B512P** **512Kb**; 3.0 V 40-MHz SPI; Ind RTC	**CY14B512I** **512Kb**; 3.0 V 3.4-MHz I²C; Ind RTC	
64Kb–256Kb		**CY14B256KA/LA** **256Kb**; 3.0 V 25, 45 ns; x8; Ind RTC	**CY14V/U256LA** **256Kb**; 3.0, 1.8 V I/O 35 ns; x8; Ind					
		Q323 **CY14E256LA** **256Kb**; 5.0 V 25, 45 ns; x8; Ind			**CY14B256PA** **256Kb**; 3.0 V 40-MHz SPI; Ind RTC		**CY14B256I** **256Kb**; 3.0 V 3.4-MHz I²C; Ind RTC	
					CY14B064PA **64Kb**; 3.0 V 40-MHz SPI; Ind RTC		**CY14B064I** **64Kb**; 3.0 V 3.4-MHz I²C; Ind RTC	

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY
EOL (Last-Time-Ship)				QQYY
Automotive				

[1] Low-pin-count
[2] Industrial grade -40 °C to +85 °C
[3] Real-time clock
[4] Open NAND flash interface
[5] Error-correcting code
[6] AEC-Q100 -40 °C to +125 °C
[7] Quad serial peripheral interface
[8] Extended Industrial grade -40 °C to +105 °C
[9] Military grade -55 °C to +125 °C

Nonvolatile RAM roadmap

Product Family	Density (ES) [EOL]	2021				2022				2023				2024				2025			
		Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Serial EXCELON™ F-RAM QSPI, SPI 1.71–1.89 V 1.8–3.6 V	Ultra																				
	Auto																				
	LP																				
Serial F-RAM SPI, I^2C 3.3/5 V	4Kb–4Mb																				
Processor Companion I^2C 3.3/5 V	64Kb, 256Kb																				
Parallel F-RAM x8, x16 3.3/5 V	64Kb–4Mb																				
Parallel nvSRAM x8, x16 3 V, 5 V	256Kb–16Mb																				
Serial nvSRAM I^2C, SPI, QSPI 3 V, 5 V	64Kb–1Mb																				

Concept Samples Production EOL

nvSRAM packages

Family	Density	8-pin SOIC	8-pin DFN	16-pin SOIC	28-pin SOIC	28-pin CDIP	28-pad LCC	32-pin SOIC	44-pin TSOP II	48-ball FBGA	48-pin SSOP	48-pin TSOP I	54-pin TSOPII	60-ball FBGA	165-ball FBGA	Wafer
Parallel	64Kb				✓	✓	✓									
	256Kb				✓	✓	✓		✓	✓	✓					
	1Mb								✓	✓	✓		✓			
	4Mb								✓	✓			✓			✓
	8Mb								✓	✓			✓			
	16Mb								✓			✓	✓	✓	✓	✓
SPI	64Kb	✓		✓												
	256Kb	✓	✓	✓												
	512Kb	✓		✓												
	1Mb	✓	✓	✓												
I²C	64Kb	✓		✓												
	256Kb			✓												
	512Kb			✓												
	1Mb	✓		✓												

Parallel asynchronous SRAM

Low-power (MoBL™), Fast asynchronous SRAM with power snooze capability

Parallel asynchronous SRAM portfolio

High density | Wide voltage range | Automotive A[1], E[2] | On-chip ECC

Density

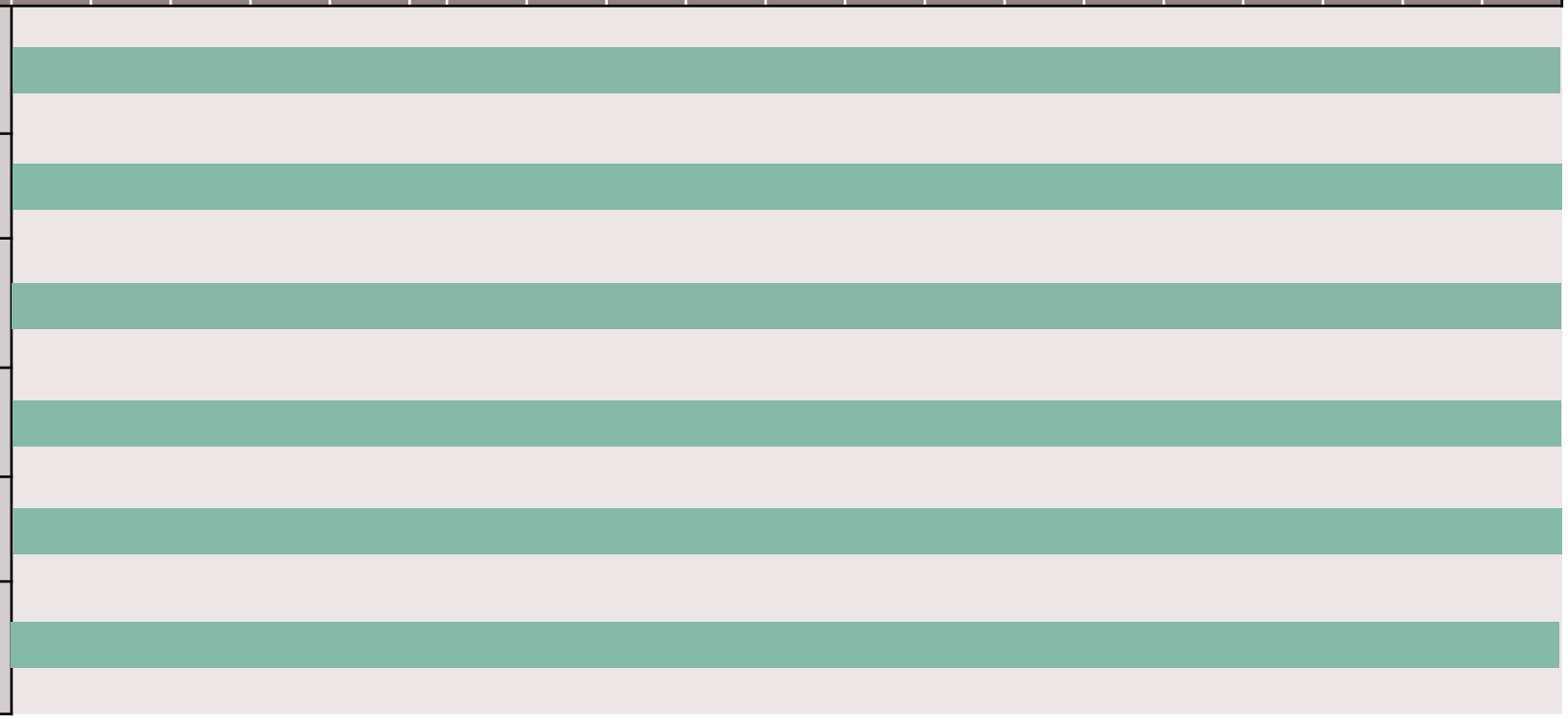
	Fast SRAM		Low-Power SRAM (MoBL™[3])			Fast SRAM with power snooze[4]
	Non-ECC (≥65 nm)	ECC (65 nm)	Non-ECC (≥90 nm)	ECC (65 nm)	ECC (65 nm) ULP[5]	ECC (65 nm)
32Mb–64Mb	**CY7C107x** **32Mb**; 3.3 V 12 ns; x8, x16 Ind		**CY6218x** **64Mb**; 1.8, 3.0 V 55 ns; x16 Ind **CY6217x** **32Mb**; 1.8-5.0 V 55 ns; x16 Ind		**CY6218x** **64Mb**; 3.0 V 55 ns; x16 Ind **CY6217x** **32Mb**; 3.0 V 55 ns; x16 Ind	
2Mb–16Mb	**CY7C106xGN** **16Mb**; 1.8, 3.3 V 10 ns; x8, x16, x32 Ind **CY7C105x** **8Mb**; 3.3 V 10 ns; x8, x16 Ind **CY7C1012** **12Mb**; 3.3 V 10 ns; x24 Ind **CY7C104x** **4Mb**; 3.3, 5.0 V 10 ns; x4, x8, x16 Ind, Auto A, E **CY7C1034** **6Mb**; 3.3 V 10 ns; x24 Ind **CY7C1010/11** **2Mb**; 3.3 V 10 ns; x8, x16 Ind, Auto A, E **CY7C1024** **3Mb**; 3.3 V 10 ns; x24 Ind	**CY7C106xG/GE** **16Mb**; 1.8-5.0 V 10 ns; x8, x16, x32 Ind, Auto E **CY7C105x** **8Mb**; 3.3, 5.0 V 10 ns; x8, x16 Ind, Auto E **CY7C104x** **4Mb**; 1.8-5.0 V 10 ns; x8, x16 Ind, Auto E	**CY6216x** **16Mb**;1.8, 3.0, 5.0 V 45 ns; x8, x16 Ind, Auto A **CY6215x** **8Mb**; 1.8, 3.0, 2.5-5.0 V 45 ns; x8, x16 Ind, Auto A, E **CY6214x** **4Mb**; 1.8, 3.0, 2.5-5.0 V 45 ns; x8, x16 Ind **CY6213x** **2Mb**; 1.8, 2.5-5.0 V 45 ns; x8, x16 Ind, Auto A, E	**CY6216x** **16Mb;** 1.8-5.0 V 45 ns; x8, x16, x32 Ind, Auto E **CY6215x** **8Mb;** 3.3, 5.0 V 45 ns; x8, x16 Ind, Auto A, E **CY6214x** **4Mb**; 1.8-5.0 V 45 ns; x8, x16 Ind, Auto A, E	**CY6216x** **16Mb;** 3.0 V 45 ns; x8, x16 Ind **CY6215x** **8Mb;** 1.8V**,** 3.0 V 45 ns; x8, x16 Ind, Auto A	**CY7S106x** **16Mb**; 1.8-5.0 V 10 ns; x8, x16, x32 Ind **CY7S104x** **4Mb**; 1.8-5.0 V 10 ns; x8, x16 Ind
64Kb–1Mb	**CY7C1020** **512Kb**; 2.6, 3.3, 5.0 V 10 ns; x16 Ind, Auto E **CY7C1019/21/100x** **1Mb**; 2.6, 3.3, 5.0 V 10 ns; x4, x8, x16 Ind, Auto A, E **CY7C19x/1399** **256Kb**; 3.3, 5.0 V 10 ns; x4, x8 Ind, Auto A		**CY6212x** **1Mb**; 2.5-5.0 V 45 ns; x8, x16 Ind, Auto A, E **CY62256** **256Kb**; 1.8, 3.0, 5.0 V 55 ns, 70 ns; x8 Ind, Auto A, E			

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY
EOL (Last-Time-Ship)				QQYY
Automotive				

[1] AEC-Q100 -40 °C to +85 °C
[2] AEC-Q100 -40 °C to +125 °C
[3] More Battery Life
[4] A Fast SRAM with a deep-sleep mode in addition to the conventional standby
[5] Ultra-Low-Power

Parallel asynchronous SRAM roadmap

Product Family	Density
MoBL™ SRAM ULP 65 nm, ECC Parallel Asynchronous	8Mb, 16Mb, 32Mb, 64Mb
MoBL™ SRAM 65 nm, ECC Parallel Asynchronous	4Mb, 8Mb, 16Mb
MoBL™ L SRAM ≥ 90 nm, Parallel Asynchronous	64Kb, 256Kb, 512Kb, 1Mb, 2Mb, 4Mb, 8Mb, 16Mb, 32Mb, 64Mb
Fast SRAM with power snooze, 65 nm, ECC Parallel Asynchronous	4Mb, 16Mb
Fast SRAM 65 nm, ECC Parallel Asynchronous	2Mb, 4Mb, 8Mb, 16Mb
Fast SRAM ≥ 90 nm Parallel Asynchronous	64Kb, 256Kb, 512Kb, 1Mb, 2Mb, 3Mb, 6Mb, 8Mb, 12Mb, 32Mb, 64Mb



Low-power SRAM family with ECC[1]

Applications

Programmable logic controllers, handheld devices, multifunction printers, implantable medical devices, computation servers, and automotive

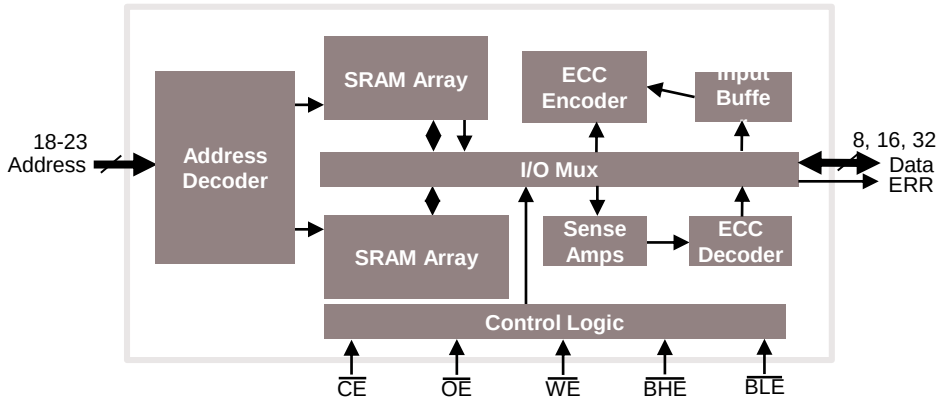
Features

- **Speed**
  - Access time: 45 ns
  - Bus-width configurations: x8, x16, and x32
- **Low power**
  - Standby current: 8.7 µA for 4Mb
- **Features**
  - ECC[1] logic to detect and correct single-bit errors
- **Multiple operating temperatures**
  - Industrial and automotive temperature grades
- **RoHS[2]-compliant packages**
  - 48-ball and 119-ball BGA
  - 32-pin and 44-pin TSOP-II
  - 48-pin TSOP-I
  - 32-pin SOIC

Collateral

Datasheet: Asynchronous SRAM with ECC

SRAM with ECC



Family table

Density	MPN	Standby Current (Maximum at 85 °C)	Standby Current (Typical at 25 °C)
4Mb	CY6214x	8.7 µA	3.5 µA
8Mb	CY6215x	16.0 µA	5.5 µA
16Mb	CY6216x	16.0 µA	5.5 µA

Availability

Production: Now

[1] Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation

[2] Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components

Ultra low-power MoBL™[1] SRAM family with ECC[2]

Applications

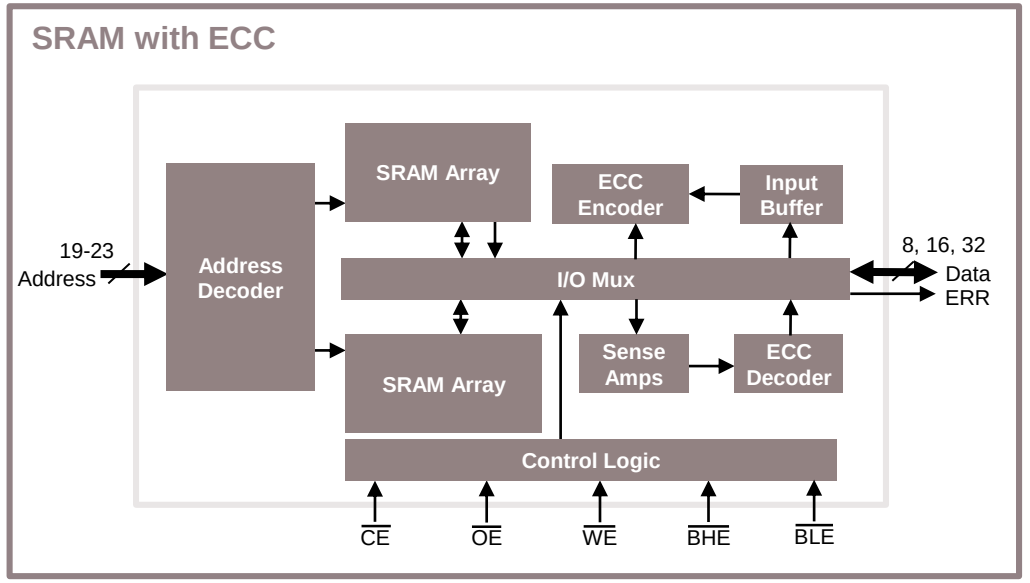
Programmable logic controllers, handheld devices, multifunction printers, implantable medical devices, automotive, and computation servers

Features

- **Speed**
  - Access time: 45/55 ns
  - Bus-width configurations: x8 and x16
- **Low power**
  - Standby current: 8.0 µA max for 16Mb
- **Operating voltage range**
  - 2.2 V to 3.6 V, 1.65V to 2.25V (8Mb)
- **Features**
  - ECC[2] logic to detect and correct single-bit errors
- **Temperature grades**
  - 8Mb, 16Mb, 32Mb, 64Mb; Industrial grade: -40 ° C to +85 ° C
  - 8Mb; Automotive A grade: -40 ° C to +85 ° C
- **RoHS[3]-compliant packages**
  - All existing MoBL™ packages supported

Collateral

Datasheet: 64Mb ULP SRAM; 32Mb ULP SRAM
16Mb ULP SRAM; 8Mb ULP SRAM



Family table

Density	MPN	Standby Current (Maximum at 85 C)	Standby Current (Typical at 25 C)
8Mb	CY6215x	6.5 µA	1.4 µA
16Mb	CY6216x	8.0 µA	1.5 µA
32Mb	CY6217x	19.0 µA	3.0 µA
64Mb	CY6218x	38.0 µA	6.0 µA

Availability

Production: Now

[1] MoBL: More Battery Life
[2] Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
[3] Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components

Fast SRAM family with ECC[1]

Applications

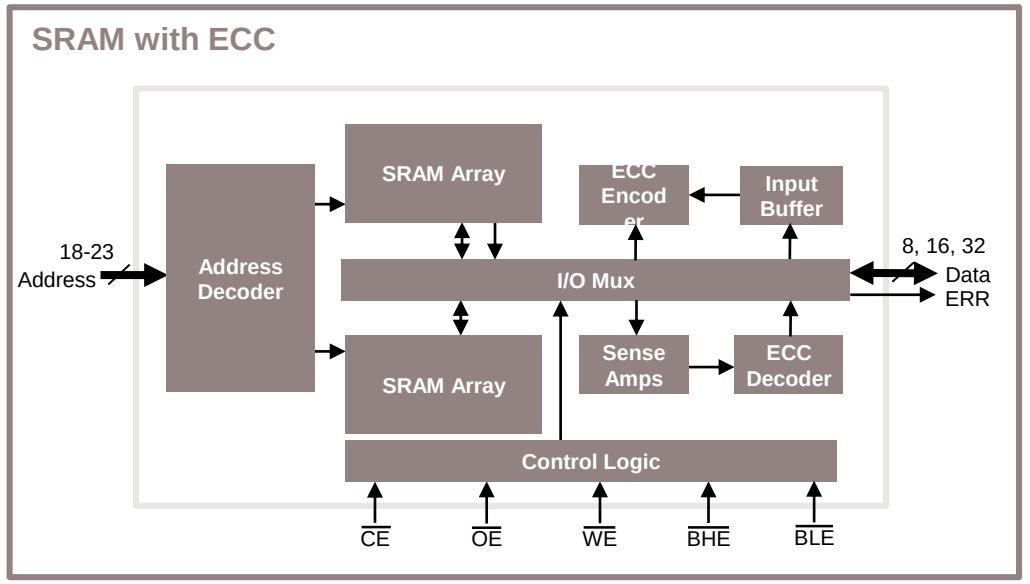
Programmable logic controllers, handheld devices, multifunction printers, implantable medical devices, automotive, and computation servers

Features

- **Speed**
  - Access time: 10 ns
  - Bus-width configurations: x8, x16 and x32
- **Features**
  - ECC[2] logic to detect and correct single-bit errors
  - Bit-interleaving to avoid multi-bit errors
  - Error indication (ERR) pin to indicate single-bit errors
- **Temperature grades**
  - Industrial grade: -40 ° C to +85 ° C
  - Automotive A grade: -40 ° C to +85 ° C
- **RoHS[2]-compliant packages**
  - 48-ball and 119-ball BGA
  - 44-pin and 54-pin TSOP-II
  - 48-pin TSOP-I
  - 34-pin and 36-pin SOJ

Collateral

Datasheet: Asynchronous SRAM with ECC



Family table

Density	MPN	Access Time	Operating Current (Maximum at 85 C
4Mb 8Mb 16Mb	CY7C104x CY7C105x CY7C106x	10 ns 10 ns 10 ns	45 mA 110 mA 110 mA

Availability

Production: Now

[1] Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation

[2] Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components

Fast SRAM family with power snooze[1] capability

Applications

Programmable logic controllers, handheld devices, multifunction printers, computation servers, and automotive

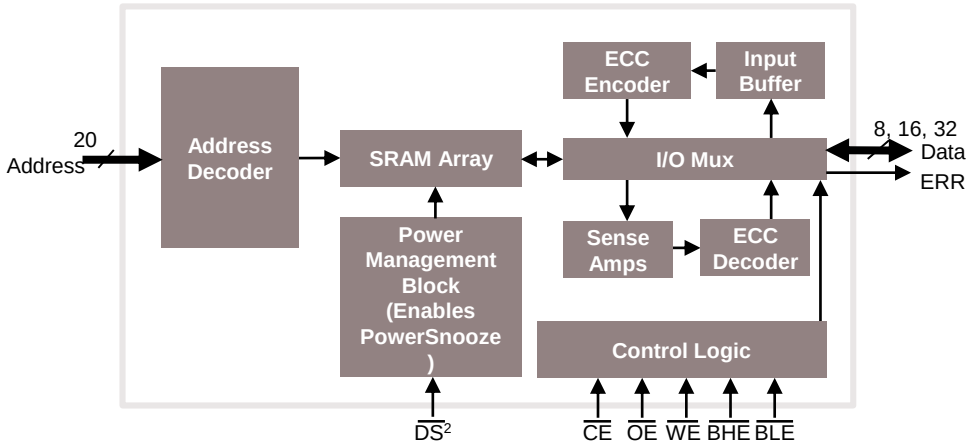
Features

- **Speed**
  - Access time: 10 ns
  - Bus-width configurations: x8, x16, and x32
- **Low power**
  - Deep-sleep current: 15 µA for 4Mb
- **Features**
  - ECC[2] logic to detect and correct single-bit errors
  - Bit-interleaving to avoid multi-bit errors
  - Error Indication (ERR) pin to indicate single-bit errors
- **Multiple operating temperatures**
  - Industrial and automotive temperature grades
- **RoHS[3]-compliant packages**
  - 48-ball BGA
  - 44-pin and 54-pin TSOP-II
  - 48-pin TSOP-I
  - 36-pin and 44-pin SOJ

Collateral

Datasheet: Asynchronous SRAM with ECC

SRAM with power snooze capability



Family table

Density	MPN	Access Time	Deep Sleep Current (Maximum at 85 °C)
4Mb	CY7S104x	10 ns	15 µA
16Mb	CY7S106x	10 ns	22 µA

Availability

Production: Now

[1] A Fast SRAM with a deep sleep mode in addition to a conventional standby mode
[2] Error-correcting code
[3] Restriction of Hazardous Substances. A European Union directive intended to eliminate the use of environmentally hazardous material in electronic components

Parallel asynchronous SRAM packages

Family	Density	28-pin TSOP I	32-pin TSOP I	48-pin TSOP I	32-pin TSOP II	44-pin TSOP II	48-pin TSOP II	54-pin TSOP II	36-ball BGA	48-ball BGA	119-ball BGA	28-pin PDIP	28-pin SOJ	32-pin SOJ	36-pin SOJ	44-pin SOJ	32-pin SOIC	28-pin SNC	60-ball CSP	Wafer
Fast	256Kb	✓											✓							✓
	512Kb					✓										✓				
	1Mb		✓		✓	✓				✓			✓	✓		✓				✓
	2Mb					✓				✓					✓					
	3Mb										✓									
	4Mb					✓				✓					✓	✓				✓
	6Mb										✓									
	8Mb					✓				✓										
	12Mb										✓									
	16Mb			✓				✓		✓	✓									
	32Mb									✓										
Low-power	256Kb	✓										✓						✓		
	1Mb		✓			✓				✓							✓			✓
	2Mb		✓		✓	✓			✓	✓							✓			✓
	4Mb		✓		✓	✓				✓							✓			✓
	8Mb			✓		✓				✓										✓
	16Mb			✓						✓	✓									✓
	32Mb			✓						✓										
	64Mb									✓										

HYPERRAM™

High-performance pseudo-static RAM

HYPERRAM™ & Octal xSPI RAM portfolio
High-performance | Low pin count | Small footprint

	HYPERRAM™ 1.0 KL-1 x8, 3.0 V HYPERBUS™ I/F	HYPERRAM™ 1.0 KS-1 x8, 1.8 V HYPERBUS™ I/F	HYPERRAM™ 2.0 KL-2 x8, 3.0 V HYPERBUS™ I/F	HYPERRAM™ 2.0 KS-2 x8, 1.8 V HYPERBUS™ I/F	Octal xSPI RAM KL-3 x8, 3.0 V Octal xSPI I/F	Octal xSPI RAM KS-3 x8, 1.8 V Octal xSPI I/F	HYPERRAM™ 3.0 KS-4 x16, 1.8 V HYPERBUS™-Ext. I/O I/F
	Density Initial Access/DDR Clock * Temperature Range						
256–512Mb				**512Mb**[1] 35 ns/200 MHz * I, A, V, B, M **256Mb** 35 ns/200 MHz * I, A, V, B, M		**512Mb**[1] 35 ns/200 MHz * I, A, V, B, M **256Mb** 35 ns/200 MHz * I, A, V, B, M	**256Mb** 35 ns/200 MHz * I, V, A, B
64–128Mb	**128Mb**[1] 40 ns/100 MHz * I, A, V, B **64Mb** 40 ns/100 MHz * I, A, V, B	**128Mb**[1] 36 ns/166 MHz * I, A, V, B **64Mb** 36 ns/166 MHz * I, A, V, B	**128Mb**[1] 35 ns/166 MHz, 200MHz * I, A, V, B, M **64Mb** 35 ns/166 MHz, 200MHz * I, A, V, B, M	**128Mb**[1] 35 ns/200 MHz * I, A, V, B, M **64Mb** 35 ns/200 MHz * I, A, V, B, M	**128Mb**[1] 35 ns/166 MHz, 200MHz * I, A, V, B **64Mb** 35 ns/166 MHz, 200MHz * I, A, V, B	**128Mb**[1] 35 ns/200 MHz * I, A, V, B **64Mb** 35 ns/200 MHz * I, A, V, B	

* I = Industrial: -40 °C to +85 °C
  A = Automotive, AEC-Q100 Grade 3: -40 °C to +85 °C
  V = Industrial-plus: -40 °C to +105 °C
  B = Automotive, AEC-Q100 Grade 2: -40 °C to +105 °C
  M = Automotive, AEC-Q100 Grade 1: -40 °C to +125 °C

[1] Stacked die

HYPERRAM™ Family Roadmap

Product Family	Density	Interface	2020				2021				2022				2023				2024			
			Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
KS-1 (1.8 V) KL-1 (3.0 V) HyperRAM 1.0 63-nm PS-RAM	128Mb[1] 64Mb	x8 HyperBus																				
KS-2 (1.8 V) KL-2 (3.0 V) HyperRAM 2.0 38-nm PS-RAM	128Mb[1] 64Mb	x8 HyperBus																				
KS-3 (1.8 V) KL-3 (3.0 V) Octal xSPI RAM 38-nm PS-RAM	128Mb[1] 64Mb	x8 Octal xSPI																				
KS-2 (1.8 V) HyperRAM 2.0 25-nm PS-RAM	512Mb[1] 256Mb	x8 HyperBus																				
KS-3 (1.8 V) Octal xSPI RAM 25-nm PS-RAM	512Mb[1] 256Mb	x8 Octal xSPI																				
KS-4 (1.8 V) HyperRAM 3.0 25-nm PS-RAM	256Mb	x16 HyperBus Extended I/O																				

Concept
Samples
Production
EOL - LTB
EOL - LTS

[1] Stacked die

HYPERRAM™ 2.0 Family

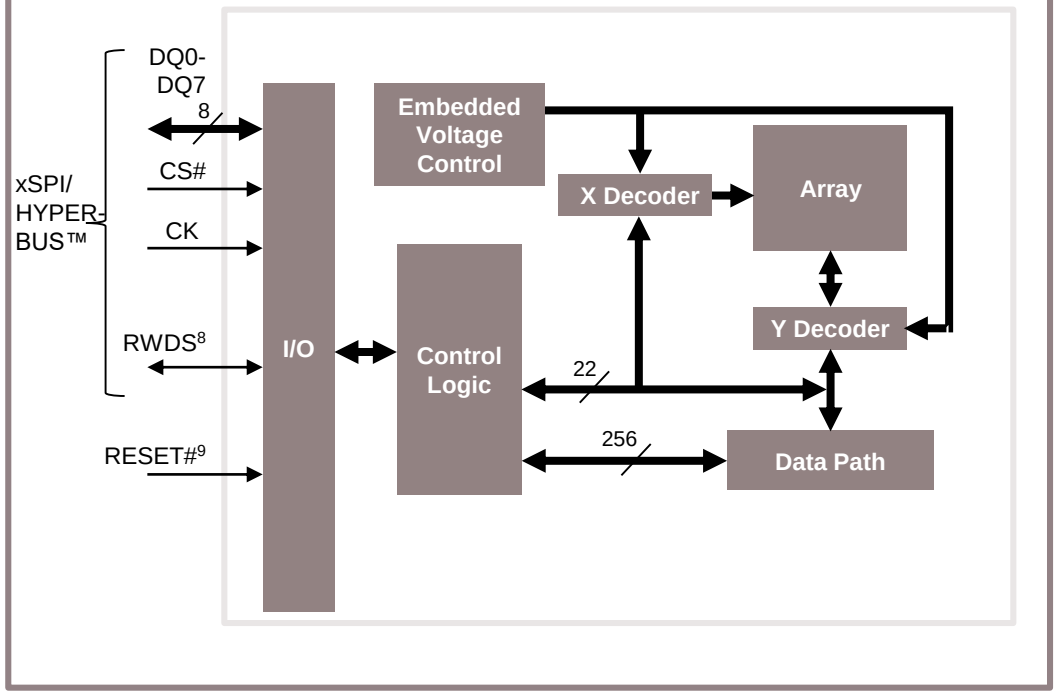
Applications

Automotive instrument clusters, Industrial HMI, industrial machine vision, and display systems in the industrial and consumer segments

Features

- Density: 64Mb, 128Mb, 256Mb, 512Mb HyperRAM[1]
- Operating voltage range: 1.7-2.0 V (64Mb, 128Mb, 256Mb, 512Mb); 2.7–3.6 V (64Mb,128Mb)
- HYPERBUS™[2] and Octal SPI interfaces compliant with JEDEC xSPI standard
- Access time: 35 ns (max), Clock rate: Up to 200 MHz
- Data bus width: x8 (64Mb, 128Mb, 256Mb, 512Mb)
- Double data rate (DDR)[3] read/write bandwidth[4]: 400 MBps (x8)
- Configurable burst modes (Linear burst, Wrapped length burst, and Hybrid burst)
- Configurable output drive strength
- Hybrid Sleep Mode and Deep Power Down Mode
  - Deep Power Down[5] :10 µA (max) and Hybrid Deep Sleep[6]: 25 µA (typ) at 85ºC for 1.8 V
  - Deep Power Down :12 µA (max) and Hybrid Deep Sleep: 35 µA (typ) at 85ºC for 3.0 V
- Active current : 25 mA (max) at 85 ºC for 1.8 V; 30 mA (max) at 85 ºC for 3.0 V
- Partial Memory Array Refresh feature to optimize battery performance
- Industrial grade (-40ºC to +85ºC) and extended-industrial grade (-40ºC to +105ºC)
- Auto Grade-1 (-40ºC to +125ºC), Grade-2 (-40ºC to +105ºC) and Grade-3 (-40ºC to +85ºC)
- Package: 24-ball BGA[7] 6 mm x 8 mm (x8); 49-ball BGA 8 mm x 8 mm (x16)
- Pin- and function-compatible products are available from multiple vendors

64Mb-512Mb x8 HYPERRAM™ Memory



Availability

Production: Now

Collateral

Datasheets: HYPERRAM 2.0

[1] A self-refresh DRAM with a HyperBus interface
[2] A high-bandwidth, 12-signal interface that transfers information over 8 I/O signals at double data rate (DDR), delivering up to 400 MBps
[3] A mode of data transfer in which data is transferred twice per clock cycle
[4] The measurement of how fast data can be read from or written to a memory, expressed in bytes per second
[5] A power-saving mode in which all sense amps and peripheral circuits are turned off
[6] A power-saving mode in which the data is retained
[7] Ball Grid Array (BGA) supports a 1-mm ball pitch
[8] Read/Write Data Strobe I/O
[9] Hardware reset input; this pin is not mandatory for data transactions. Refer to the HYPERBUS specification for more information.

HYPERRAM™ 3.0 Family

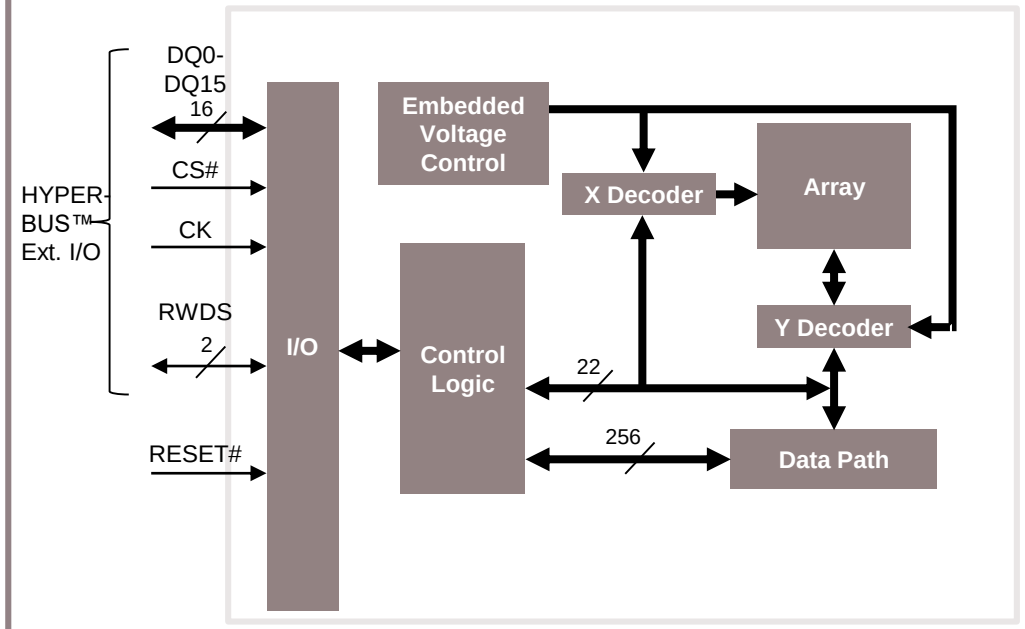
Applications

Graphics/display systems and AI applications in the industrial and consumer segments

Features

- Operating voltage range: 1.7–2.0 V
- HYPERBUS™ Extended I/O interface
- Access time: 35 ns (max), Clock rate: 200 MHz
- Data Bus Width: 16-bit (x16)
- Double data rate (DDR)[1] read/write bandwidth: 800 MBps
- Configurable burst modes (Linear burst, Wrapped length burst and Hybrid burst)
- Configurable output drive strength
- Deep Power Down Mode[2] and Hybrid Sleep Mode[3]
  - Deep Power Down:12 µA (max) and Hybrid Deep Sleep: 140 µA (typ) at 85 ºC
- Active current (Read/Write): 20/22 mA (max) at 85 ºC
- Partial Memory Array Refresh[4] feature to optimize battery performance
- Industrial grade (-40 ºC to +85 ºC), Extended-industrial grade (-40 ºC to +105 ºC) & Automotive (-40 ºC to +105 ºC)
- Package: 49-ball BGA[5] 8 mm x 8 mm
- Densities: 256Mb

256Mb x16 HYPERRAM™ Memory



Collateral

Datasheet: 256Mb (x16 HYPERBUS EXT. I/O

Availability

Production : Now

[1] A mode of data transfer in which data is transferred twice per clock cycle
[2] A power-saving mode in which all sense amps and peripheral circuits are turned off
[3] A power-saving mode in which the data is retained
[4] A power-saving mode in which all the internal voltage generators stay in low-power mode
[5] Ball Grid Array (BGA) supports a 1-mm ball pitch

Synchronous SRAM

Std Sync, NoBL (No bus latency), QDR™-II, DDR-II, QDR™-IV

Synchronous SRAM portfolio
High random transaction rate (RTR)[1] | Low latency | High bandwidth

Standard Sync and NoBL	Standard Sync and NoBL with ECC[2]	QDR™-II/ DDR-II	QDR™-II+/ DDR-II+	QDR™-II+X/ DDR-II+X	QDR™-IV
RTR: 250 MT/s (max.) BW: 18 Gbps (max.) Latency: 1 Cycle Pipeline and Flow-Through Modes	RTR: 250 MT/s (max.) BW: 18 Gbps (max.) Latency: 1 Cycle Pipeline and Flow-Through Modes	RTR: 666 MT/s (max.) BW: 47.9 Gbps (max.) Latency: 1.5 Cycles CIO[3] and SIO[4]	RTR: 666 MT/s (max.) BW: 79.2 Gbps (max.) Latency: 2 or 2.5 Cycles CIO and SIO, ODT[5]	RTR: 900 MT/s (max.) BW: 91.1 Gbps (max.) Latency: 2.5 Cycles SIO, ODT	RTR: 2.1 GT/s (max.) BW: 153.5 Gbps (max.) Latency: 5 or 8 Cycles Dual-Port Bidirectional ODT
		CY7C161/2xKV18 **144Mb**; 250–333 MHz 1.8 V; x9, x18, x36 Burst 2, 4	**CY7Cx4/5/6/7xKV18** **144Mb**; 300–550 MHz 1.8 V; x18, x36 Burst 2, 4		**CY7C41xKV13** **144Mb**; 667–1,066 MHz 1.3 V; x18, x36 Burst 2
CY7C147/8xB **72Mb**; 133–250 MHz 2.5, 3.3 V; x18, x36		**CY7C151/2xKV18** **72Mb**; 250–333 MHz 1.8 V; x9, x18, x36 Burst 2, 4	**CY7Cx54/5/6/7KV18** **72Mb**; 250–550 MHz 1.8 V; x18, x36 RH[6]; Burst 2, 4	**CY7C156/7xXV18** **72Mb**; 366–633 MHz 1.8 V; x18, x36 Burst 2, 4	**CY7C40xKV13** **72Mb**; 667–1,066 MHz 1.3 V; x18, x36 Burst 2
CY7C144/6xK **36Mb**; 133–250 MHz 2.5, 3.3 V; x36, x72	**CY7C144/6xKVE** **36Mb**; 133–250 MHz 2.5, 3.3 V; x18, x36	**CY7C141/2xKV18** **36Mb**; 250–333 MHz 1.8 V; x8, x9, x18, x36 Burst 2, 4	**CY7Cx24/5/6/7xKV18** **36Mb**; 400–550 MHz 1.8 V; x18, x36 Burst 2, 4	**CY7C126/7x** **36Mb**; 366–633 MHz 1.8 V; x18, x36 Burst 2, 4	
CY7C137/8xD/K **18Mb**; 100–250 MHz 3.3 V; x18, x32, x36	**CY7C137/8xKVE** **18Mb**; 100–250 MHz 2.5, 3.3 V; x18, x36	**CY7C131/2/9xKV18** **18Mb**; 250–333 MHz 1.8 V; x8, x18, x36 Burst 2, 4	**CY7Cx14/5/6/7xKV18** **18Mb**; 400–550 MHz 1.8 V; x18, x36 Burst 2, 4		
CY7C135/6xC **9Mb**; 100–250 MHz 3.3 V; x18, x32, x36 Auto E[7]		**CY7C1911xKV18** **18Mb**; 250–333 MHz 1.8 V; x9 Burst 2, 4			
CY7C134/2xG **2–4Mb**; 100–250 MHz 3.3 V; x18, x32, x36					

Density

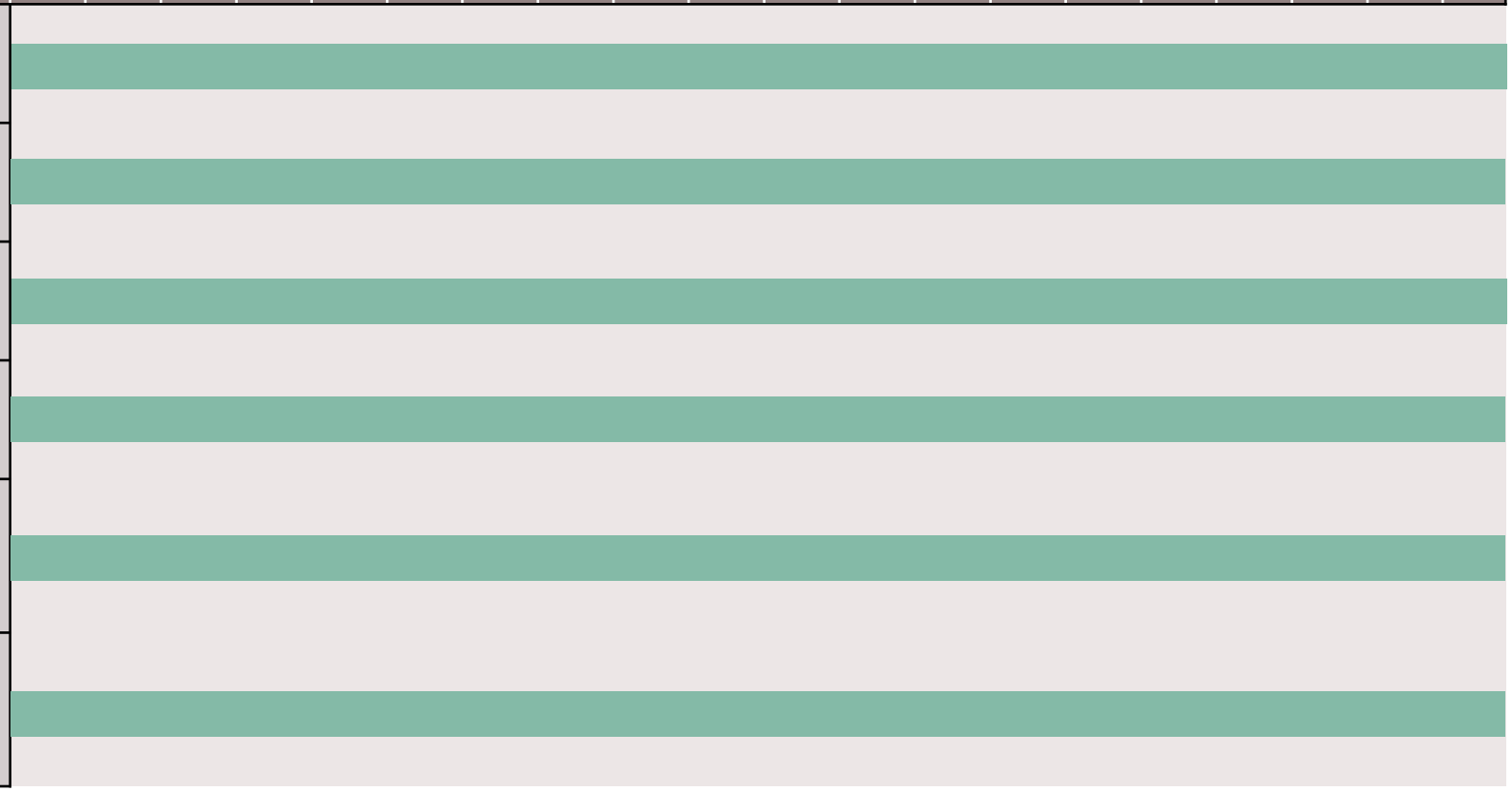
Random Transaction Rate

	Concept	Development	Sampling	Production
Status				
Availability			QQYY	QQYY
EOL (Last-Time-Ship)				QQYY
Automotive				

[1] Rate of truly random accesses to memory, expressed in transactions per second (MT/s, GT/s)
[2] Error-correcting code
[3] Common I/O
[4] Separate I/O
[5] On-die termination
[6] Radiation hardened, military grade
[7] AEC-Q100: -40 °C to +125 °C

Synchronous SRAM roadmap

Product Family	Density (Prod) [EOL]
QDR™-IV SRAM 65 nm, ECC 2.1 GT/s, 153.5 Gbps	72Mb, 144Mb
QDR™-II+X SRAM 65 nm, ECC 900 MT/s, 91.1 Gbps	36Mb, 72Mb
QDR™-II+ SRAM 65 nm, ECC 666 MT/s, 79.2 Gbps	18Mb, 36Mb, 72Mb[1], 144Mb
QDR™-II SRAM 65 nm 666 MT/s, 47.9 Gbps	18Mb, 36Mb, 72Mb, 144Mb
Standard Sync and NoBL SRAM 65 nm, ECC 250 MT/s, 18 Gbps	18Mb, 36Mb
Standard Sync and NoBL SRAM 65 nm/90 nm 250 MT/s, 18 Gbps	2Mb, 4Mb, 9Mb[2], 18Mb[3], 36Mb[3], 72Mb



[1] Radiation hardened, military grade
[2] AEC-Q100 -40 °C to +125 °C
[3] 65-nm

Standard synchronous SRAM with on-chip ECC[1]

Applications

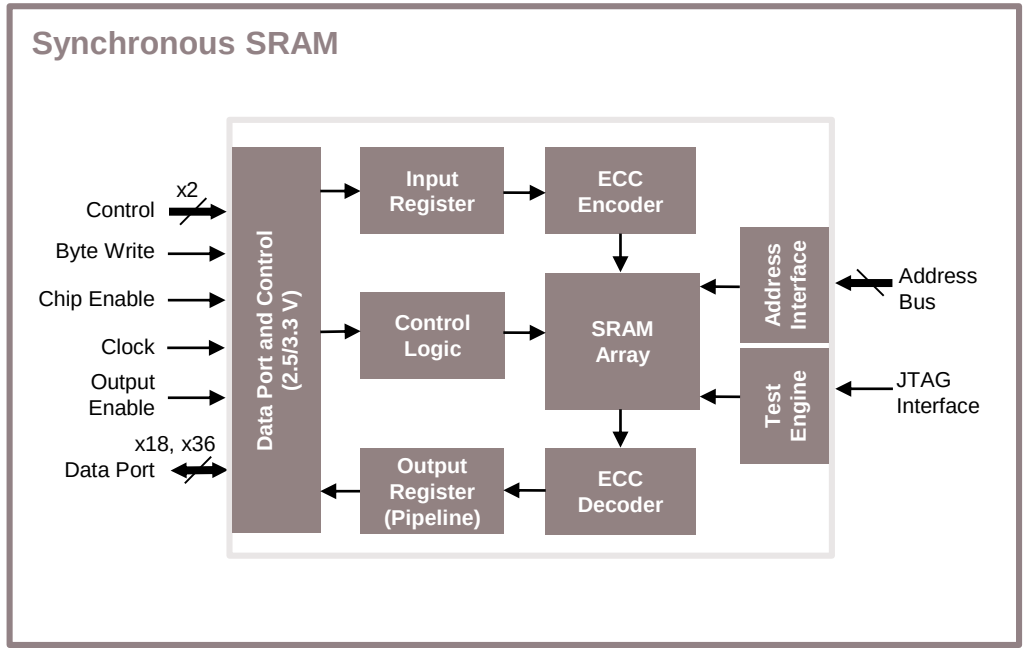
Switches and routers, radar and signal processing, test equipment, automotive, military, and aerospace systems

Features

- **Speed**
  - Available in two modes[2]: Pipeline and flow-through
  - Bus widths: x18 and x36
- **Features**
  - ECC to detect and correct single-bit errors
  - Two voltage options: 2.5 V and 3.3 V
  - SCD and DCD deselect options[3]
  - Industrial and commercial temperature grades
- **Packages**
  - 165-ball BGA
  - 100-pin TQFP

Collateral

Datasheets: 36M Sync SRAM, 18M Sync SRAM



Family Table

Option	Density	MPN	RTR	FIT/Mb[4]
Standard Sync with On-Chip ECC Pipeline	18Mb 36Mb	CY7C1370/2K CY7C1440/2K	250 MT/s	<0.01
Standard Sync with On-Chip ECC Flow-Through	18Mb 36Mb	CY7C1371/3K CY7C1441/3K	133 MT/s	<0.01

Availability

Production: Now

[1] Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
[2] Modes of synchronous SRAM operation that optimize either read latency (Flow-Through) or operating frequency (Pipeline)
[3] Modes of operation in Pipeline mode where the output driver is tri-stated after either a single cycle (SCD) or dual cycle (DCD) of issuing the deselect command
[4] The projected failure rate of a device; one FIT/Mb equals one failure per billion device hours per megabit of data

[1] Quad SPI has 4 I/Os

NoBL SRAM with on-chip ECC[1]

Applications

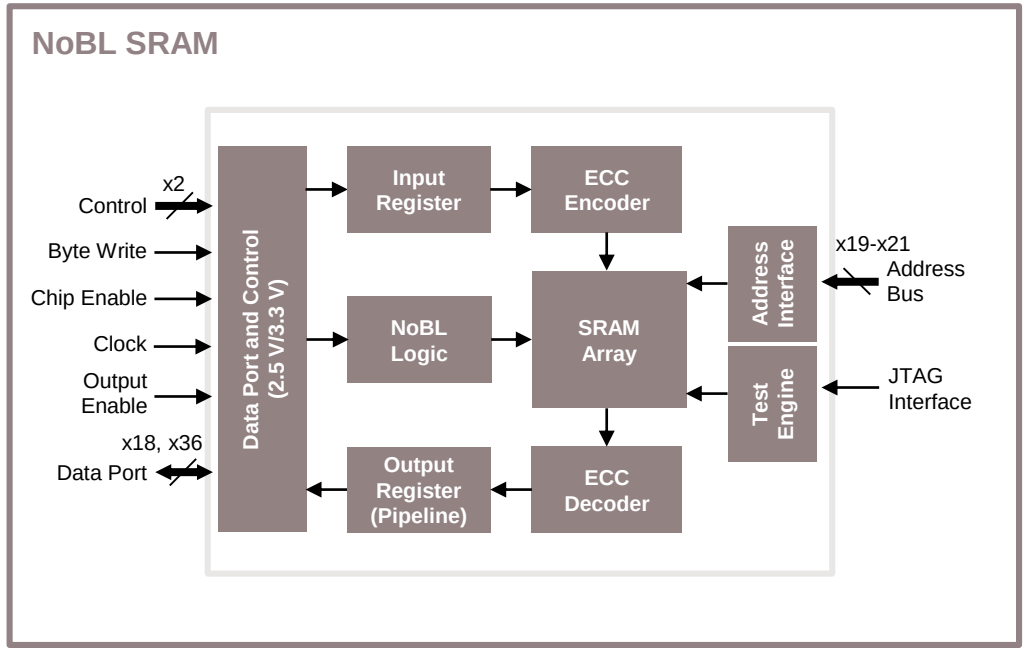
Switches and routers, radar and signal processing, test equipment, automotive, military, and aerospace systems

Features

- **Speed**
  - Available in two modes[2]: Pipeline and flow-through
  - Bus widths: x18 and x36
- **Features**
  - ECC to detect and correct single-bit errors
  - Two voltage options: 2.5 V and 3.3 V
  - SCD and DCD deselect options[3]
  - Industrial and commercial temperature grades
- **Packages**
  - 165-ball BGA
  - 100-pin TQFP

Collateral

Datasheets: 36M Sync SRAM, 18M Sync SRAM



Family Table

Option	Density	MPN	RTR	FIT/Mb[4]
NoBL with On-Chip ECC Pipeline	18Mb 36Mb	CY7C1380/2K CY7C1460/2K	250 MT/s	<0.01
NoBL with On-Chip ECC Flow-Through	18Mb 36Mb	CY7C1381/3K CY7C1461/3K	133 MT/s	<0.01

Availability

Production: Now

[1] Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors, including unavoidable errors due to background radiation
[2] Modes of synchronous SRAM operation that optimize either read latency (Flow-Through) or operating frequency (Pipeline)
[3] Modes of operation in Pipeline mode where the output driver is tri-stated after either a single cycle (SCD) or dual cycle (DCD) of issuing the deselect command
[4] The projected failure rate of a device; one FIT/Mb equals one failure per billion device hours per megabit of data

[1] Quad SPI has 4 I/Os

QDR™-IV SRAM

Applications

Switches and routers, high-performance computing, military and aerospace systems, test and measurement

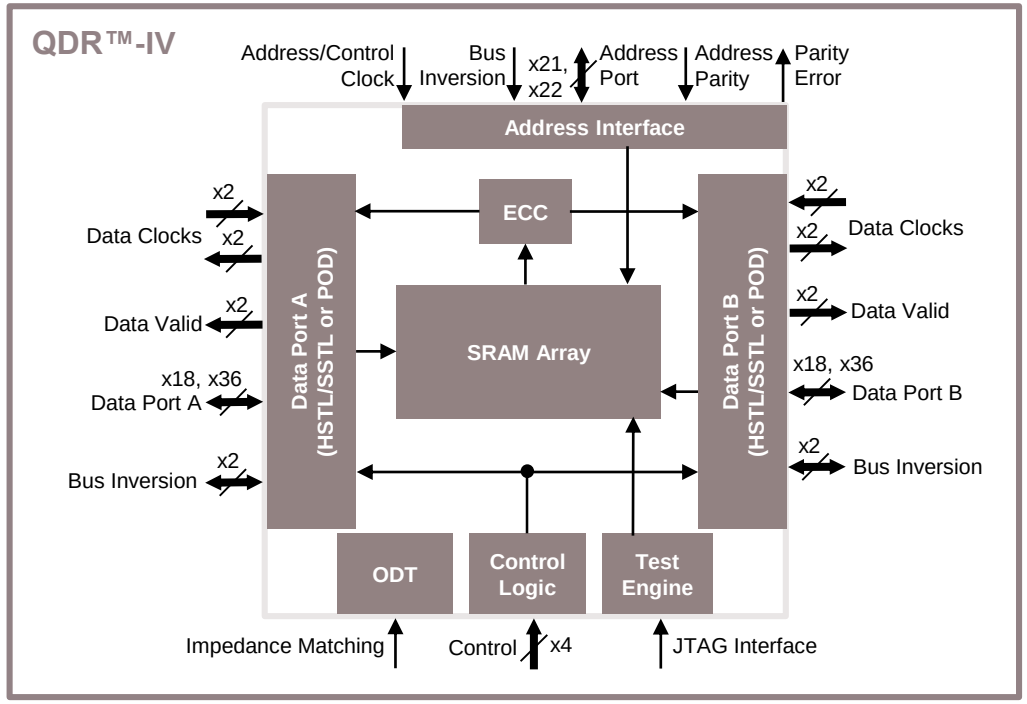
Features

- **Speed**
  - Available in two options: QDR-IV HP (RTR 1,334 MT/s) and QDR-IV XP (RTR 2,132 MT/s)
  - Two independent, bidirectional DDR[1] data ports
  - Bus widths: x18 and x360.13
- **Features**
  - ECC[2] to reduce soft error rate to less than 0.01 FIT/Mb[3]
  - Bus inversion to reduce simultaneous switching I/O noise
  - On-die termination (ODT) to reduce board complexity
  - De-skew training[4] to improve signal-capture timing
  - I/O levels: 1.2–1.25 V (HSTL/SSTL) and 1.1–1.2 V (POD[5])
- **Package**
  - 361-pin FCBGA[6]

Collateral

Datasheets: CY7C4122KV13/CY7C4142KV13
CY7C4121KV13/CY7C4141KV13
CY7C4022KV13/CY7C4042KV13
CY7C4021KV13/CY7C4041KV13

[1] Double data rate: Two data transfers per clock cycle
[2] Error-correcting code: Data encoded with extra parity bits to detect and correct bit errors
[3] Failures in Time per Megabit
[4] An iterative algorithm for assessing and eliminating the skew between multiple data signals
[5] Pseudo open drain: Signaling interface that uses strong pull-down and weak pull-up drive strength
[6] Flip-Chip Ball Grid Array



Family Table

Option	Density	MPN	Maximum Frequency	RTR
QDR-IV HP	72Mb 144Mb	CY7C40x1KV13 CY7C41x1KV13	667 MHz	1,334 MT/s
QDR-IV XP	72Mb 144Mb	CY7C40x2KV13 CY7C41x2KV13	1,066 MHz	2,132 MT/s

Availability

Production: Now

[1] Quad SPI has 4 I/Os

Synchronous SRAM packages

Family	Density	100-pin TQFP	119-ball BGA	165-ball BGA	209-ball BGA	361-ball BGA	Wafer
Std Sync	18Mb	✓		✓			
	36Mb			✓			
NoBL	2Mb	✓					
	4Mb	✓	✓				
	9Mb	✓	✓	✓			✓
	18Mb	✓	✓	✓			
	36Mb	✓		✓			✓
	72Mb	✓		✓	✓		✓
QDR	9Mb			✓			
	18Mb			✓			
	36Mb			✓			
	72Mb			✓		✓	
	144Mb			✓		✓	

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