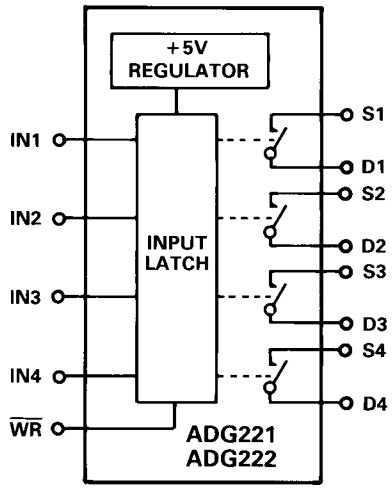
LC²MOS Quad SPST Switches

ADG221/ADG222

FEATURES

- 44V Supply Maximum Rating
- ±15V Analog Signal Range
- Low R_{ON} (60Ω)
- Low Leakage (0.5nA)
- Break-Before-Make Switching
- Extended Plastic Temperature Range (−40°C to +85°C)
- Low Power Dissipation (25.5mW)
- µP, TTL, CMOS Compatible
- Available in 16-Lead DIP/SOIC and 20-Lead PLCC/LCCC Packages
- Surface Mount Packages
- Superior DG221 Replacement

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG221 and ADG222 are monolithic CMOS devices comprising four independently selectable switches. On-chip latches facilitate microprocessor interfacing. They are designed on an enhanced LC²MOS process which gives an increased signal handling capability of ±15V. These switches also feature high switching speeds and low R_{ON}.

The ADG221 and ADG222 consist of four SPST switches. They differ only in that the digital control logic is inverted. All devices exhibit break before make switching action. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Easily Interfaced:
   Digital inputs are latched with a $\overline{WR}$ signal for microprocessor interfacing. A 5V regulated supply is internally generated permitting wider tolerances on the supplies without affecting the TTL digital input switching levels.
2. Single Supply Operation:
   For applications where the analog signal is unipolar (0V to 15V), the switches can be operated from a single +15V supply.
3. Low Leakage:
   Leakage currents in the range of 500pA make these switches suitable for high precision circuits. The added feature of Break-before-Make switching allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

$\overline{WR}$	ADG221 IN	ADG222 IN	SWITCH CONDITION
0	0	1	ON
0	1	0	OFF
1	X	X	Retains Previous Switch Condition

Table I. Truth Table

REV. B

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ADG221/ADG222—SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V, unless otherwise specified)

Parameter	K Version 25°C	K Version −40°C to +85°C	B Version 25°C	B Version −40°C to +85°C	T Version 25°C	T Version −55°C to +125°C	Units	Test Conditions
ANALOG SWITCH								
Analog Signal Range	±15	±15	±15	±15	±15	±15	Volts	
R_{ON}	60		60		60		Ω typ	$-10V \leq V_S \leq +10V$
	90	145	90	145	90	145	Ω max	I_{DS} = 1.0mA
								Test Circuit 1
R_{ON} vs. V_D (V_S)	20		20		20		% typ	
R_{ON} Drift	0.5		0.5		0.5		%/°C typ	
R_{ON} Match	5		5		5		% typ	V_S = 0V, I_{DS} = 1mA
I_S (OFF)	0.5		0.5		0.5		nA typ	V_D = ±14V; V_S ∓14V; Test Circuit 2
OFF Input Leakage	2	100	2	100	1	100	nA max	
I_D (OFF)	0.5		0.5		0.5		nA typ	V_D = ±14V; V_S = ∓14V; Test Circuit 2
OFF Output Leakage	2	100	2	100	1	100	nA max	
I_D (ON)	0.5		0.5		0.5		nA typ	V_D = ±14V; Test Circuit 3
ON Channel Leakage	2	200	2	200	1	200	nA max	
DIGITAL CONTROL								
V_{INH}, Input High Voltage		2.4		2.4		2.4	V min	
V_{INL}, Input Low Voltage		0.8		0.8		0.8	V max	
I_{INL} or I_{INH}		1		1		1	μA max	
DYNAMIC CHARACTERISTICS								
t_{OPEN}	30		30		30		ns typ	
t_{ON}[1]	300		300		300		ns max	Test Circuit 4
t_{OFF}[1]	250		250		250		ns max	Test Circuit 4
t_W[1] Write Pulse Width		100		100	100	120	ns min	See Figure 2
t_S[1] Digital Input Setup Time		100		100	100	120	ns min	See Figure 2
t_H[1] Digital Input Hold Time		20		20	20	20	ns min	See Figure 2
OFF Isolation	80		80		80		dB typ	V_S = 10V (p-p); f = 100kHz
								R_L = 75Ω; Test Circuit 6
Channel-to-Channel Crosstalk	80		80		80		dB typ	Test Circuit 7
C_S (OFF)	5		5		5		pF typ	
C_D (OFF)	5		5		5		pF typ	
C_D, C_S (ON)	16		16		16		pF typ	
C_{IN} Digital Input Capacitance	5		5		5		pF typ	
Q_{INJ} Charge Injection	20		20		20		pC typ	R_S = 0Ω; C_L = 1000pF; V_S = 0V
								Test Circuit 5
POWER SUPPLY								
I_{DD}	0.6		0.6		0.6		mA typ	Digital Inputs = V_{INL} or V_{INH}
I_{DD}		1.5		1.5		1.5	mA max	
I_{SS}	0.1		0.1		0.1		mA typ	
I_{SS}		0.2		0.2		0.2	mA max	
Power Dissipation		25.5		25.5		25.5	mW max	

NOTE
[1]Sample tested at 25°C to ensure compliance.
t_{ON}, t_{OFF} are the same for both IN and $\overline{WR}$ digital input changes.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

V_{DD} to V_{SS} 44V
V_{DD} to GND 25V
V_{SS} to GND . . . . . −25V
Analog Inputs[1]
  Voltage at S, D . . . . . V_{SS} −0.3V to V_{DD} +0.3V
  Continuous Current, S or D 30mA
  Pulsed Current S or D
    1ms Duration, 10% Duty Cycle 70mA
Digital Inputs[1]
  Voltage at IN, $\overline{WR}$ . . . . . V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First
Power Dissipation (Any Package)
  Up to +75°C 470mW
  Derates above +75°C by . . . . . 6mW/°C
Operating Temperature
  Commercial (K Version) . . . . . −40°C to +85°C
  Industrial (B Version) . . . . . −40°C to +85°C
  Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +300°C

NOTE
[1]Overvoltage at IN, $\overline{WR}$, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
ADG221KN	−40°C to +85°C	N-16
ADG221KR	−40°C to +85°C	R-16A
ADG221KP	−40°C to +85°C	P-20A
ADG221BQ	−40°C to +85°C	Q-16
ADG221TQ	−55°C to +125°C	Q-16
ADG221TE	−55°C to +125°C	E-20A
ADG222KN	−40°C to +85°C	N-16
ADG222KR	−40°C to +85°C	R-16A
ADG222KP	−40°C to +85°C	P-20A
ADG222BQ	−40°C to +85°C	Q-16
ADG222TQ	−55°C to +125°C	Q-16
ADG222TE	−55°C to +125°C	E-20A

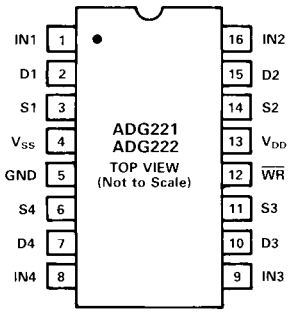
NOTES

[1]To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers. See Analog Devices Military Products Databook (1990) for military data sheet.

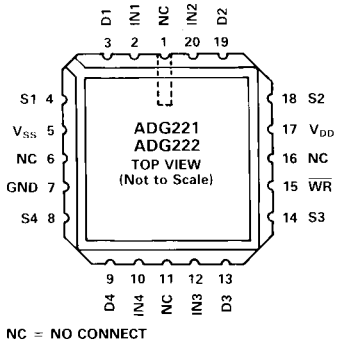
[2]N = Plastic DIP; R = 0.15" Small Outline IC (SOIC); P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; E = Leadless Ceramic Chip Carrier (LCCC).

PIN CONFIGURATIONS

DIP, SOIC

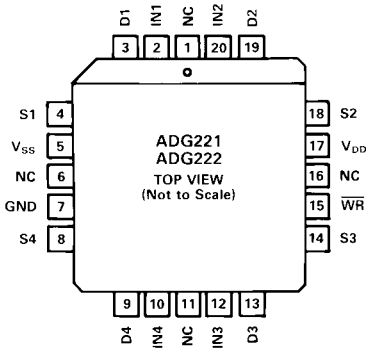


LCCC



NC = NO CONNECT

PLCC



NC = NO CONNECT

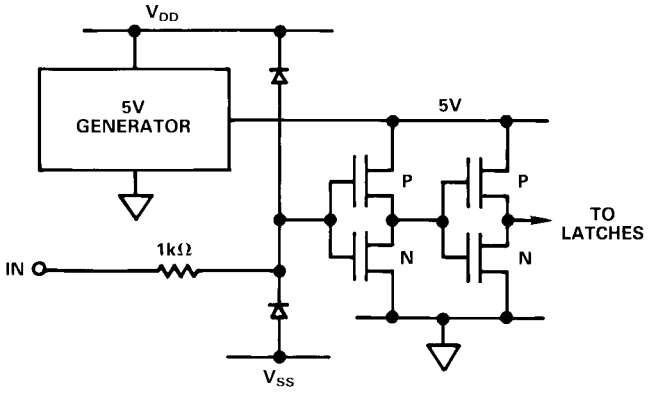
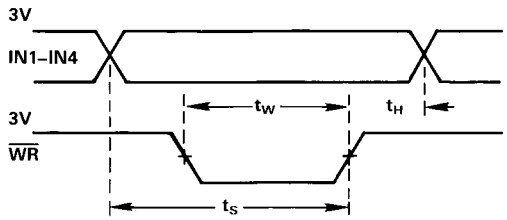


Figure 1. Typical Digital Input Cell

TIMING AND CONTROL SEQUENCE

Figure 2 shows the timing sequence for latching the switch digital inputs (IN1 – IN4). The latches are level sensitive and, therefore, while $\overline{WR}$ is held low the latches are transparent and the switches respond to the digital inputs. The digital inputs are latched on the rising edge of $\overline{WR}$.

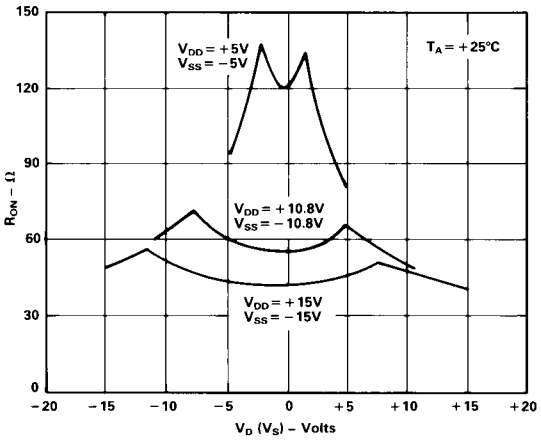


t_H – IN1–IN4 VALID TO $\overline{WR}$ HOLD TIME
t_S – IN1–IN4 VALID TO $\overline{WR}$ SETUP TIME
t_W – $\overline{WR}$ PULSE WIDTH

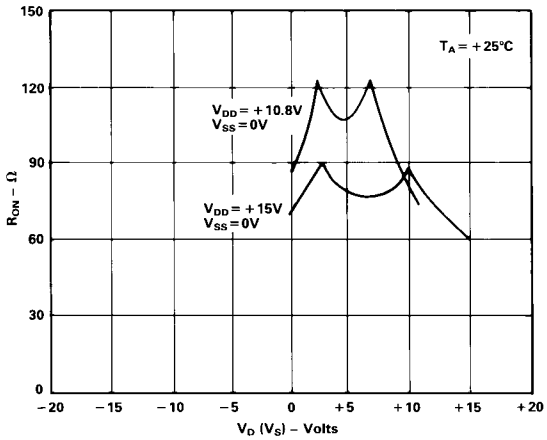
Figure 2. Timing and Control Sequence

ADG221/ADG222—Typical Performance Characteristics

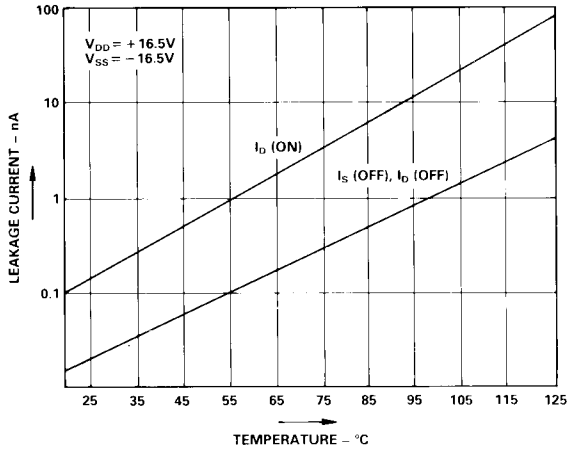
The switches are guaranteed functional with reduced single or dual supplies down to 4.5V.



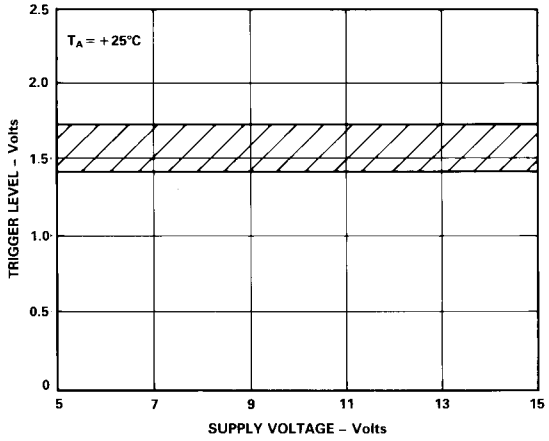
R_{ON} as a Function of V_D (V_S): Dual Supply Voltage



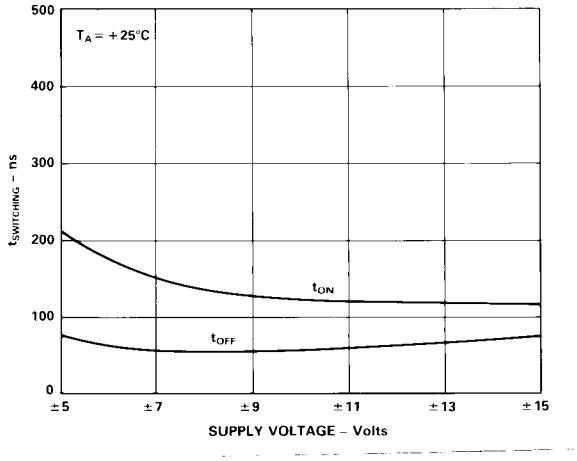
R_{ON} as a Function of V_D (V_S): Single Supply Voltage



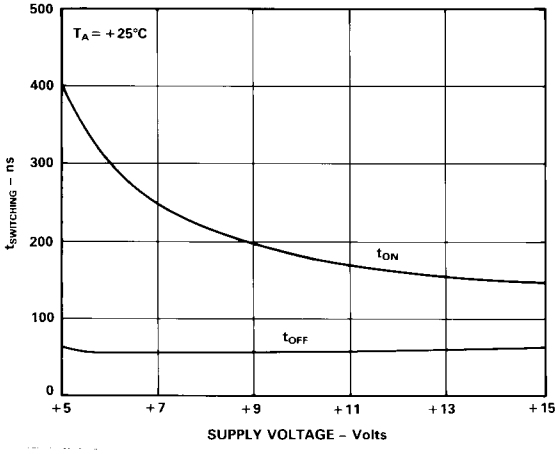
Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)



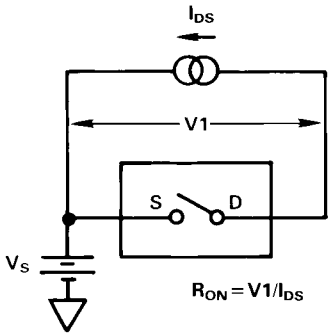
Trigger Level vs. Power Supply Voltage: Dual or Single Supply Voltage



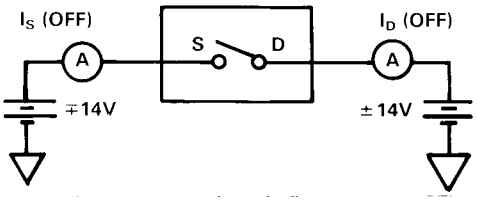
Switching Times vs. Supply Voltage (Dual Supply)



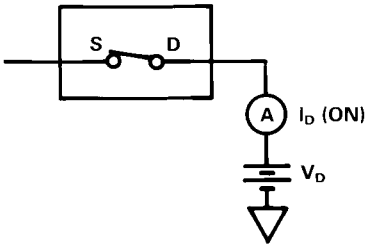
Switching Times vs. Supply Voltage (Single Supply)



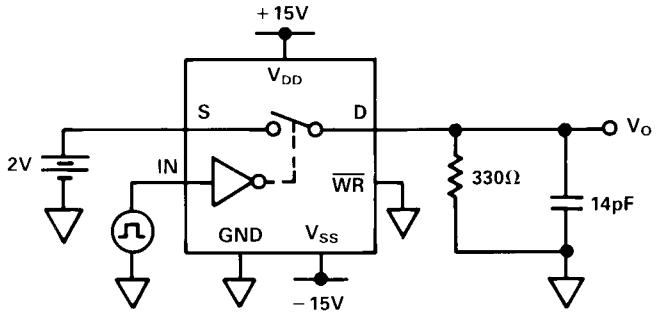
Test Circuit 1

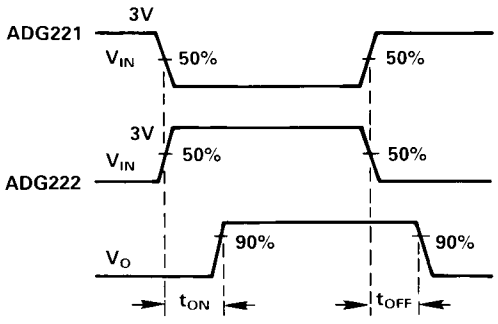


Test Circuit 2

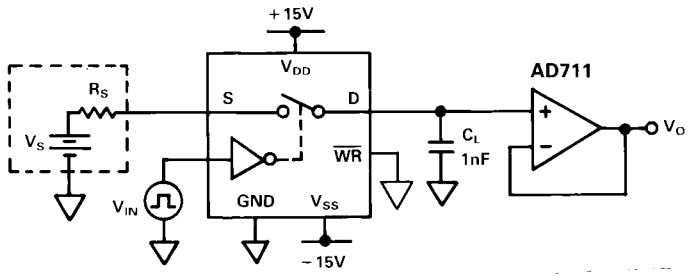


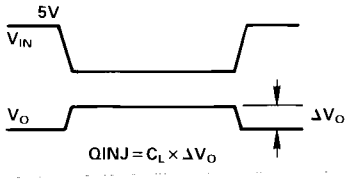
Test Circuit 3



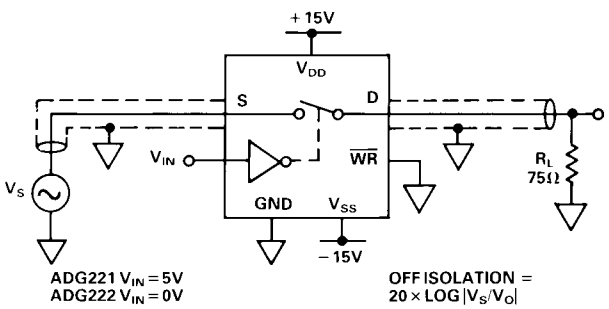


Test Circuit 4

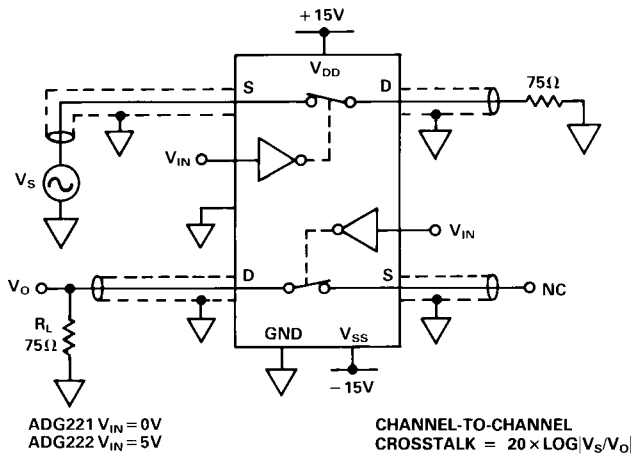




Test Circuit 5. Charge Injection



Test Circuit 6. Off Isolation



Test Circuit 7. Channel-to-Channel Crosstalk

TERMINOLOGY

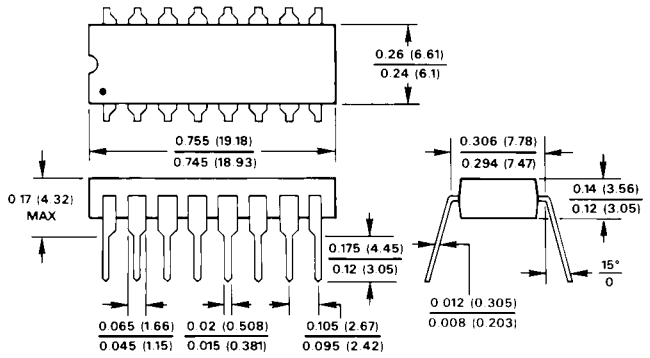
R_{ON}	Ohmic resistance between terminals OUT and S
R_{ON} Match	Difference between the R_{ON} of any two channels
I_S (OFF)	Source terminal leakage current when the switch is off
I_D (OFF)	Drain terminal leakage current when the switch is off
I_D (ON)	Leakage current that flows from the closed switch into the body
V_D (V_S)	Analog voltage on terminal D, S
C_S (OFF)	Switch input capacitance "OFF" condition
C_D (OFF)	Switch output capacitance "OFF" condition
C_{IN}	Digital input capacitance
C_D, C_S (ON)	Input or output capacitance when the switch is on
t_{ON}	Delay time between the 50% and 90% points of the digital input and switch "ON" condition
t_{OFF}	Delay time between the 50% and 90% points of the digital input and switch "OFF" condition
t_{OPEN}	"OFF" time measured between 50% points of both switches, which are connected as a multiplexer, when switching from one address state to another
V_{INL}	Maximum Input Voltage for a Logic Low
V_{INH}	Minimum Input Voltage for a Logic High
I_{INL} (I_{INH})	Input current of the digital input
V_{DD}	Most positive voltage supply
V_{SS}	Most negative voltage supply
I_{DD}	Positive supply current
I_{SS}	Negative supply current

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OUTLINE DIMENSIONS

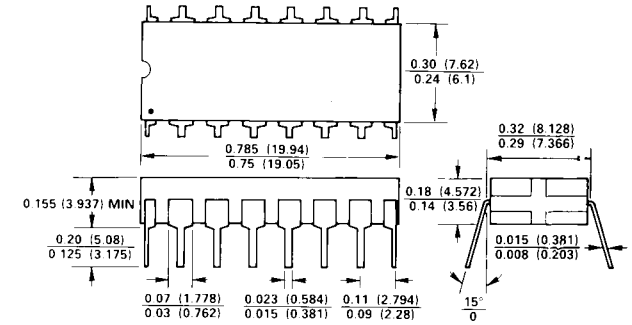
Dimensions shown in inches and (mm).

16-Pin Plastic (N-16)

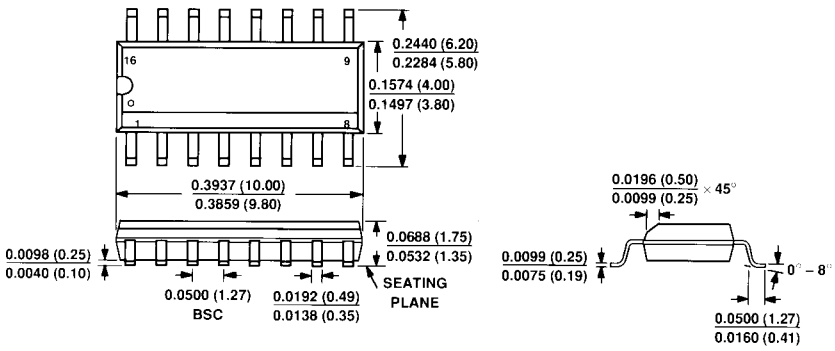


LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

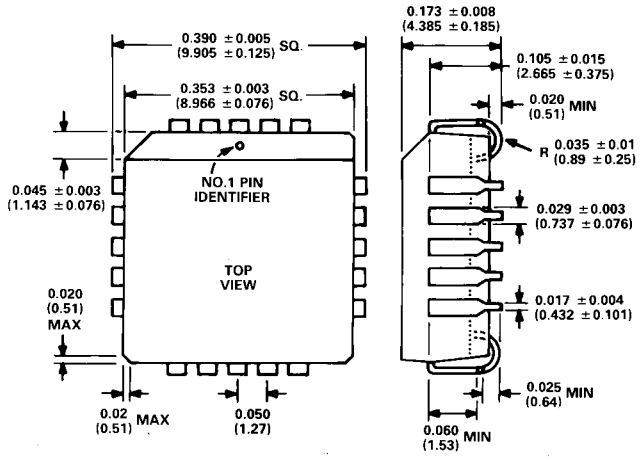
16-Pin Cerdip (Q-16)



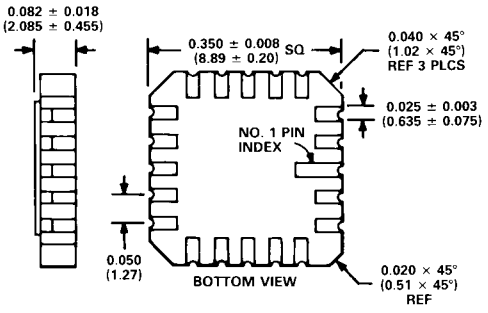
16-Lead Narrow Body SOIC (R-16A)



20-Terminal Plastic Leaded Chip Carrier (P-20A)



20-Terminal Leadless Ceramic Chip Carrier (E-20A)



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